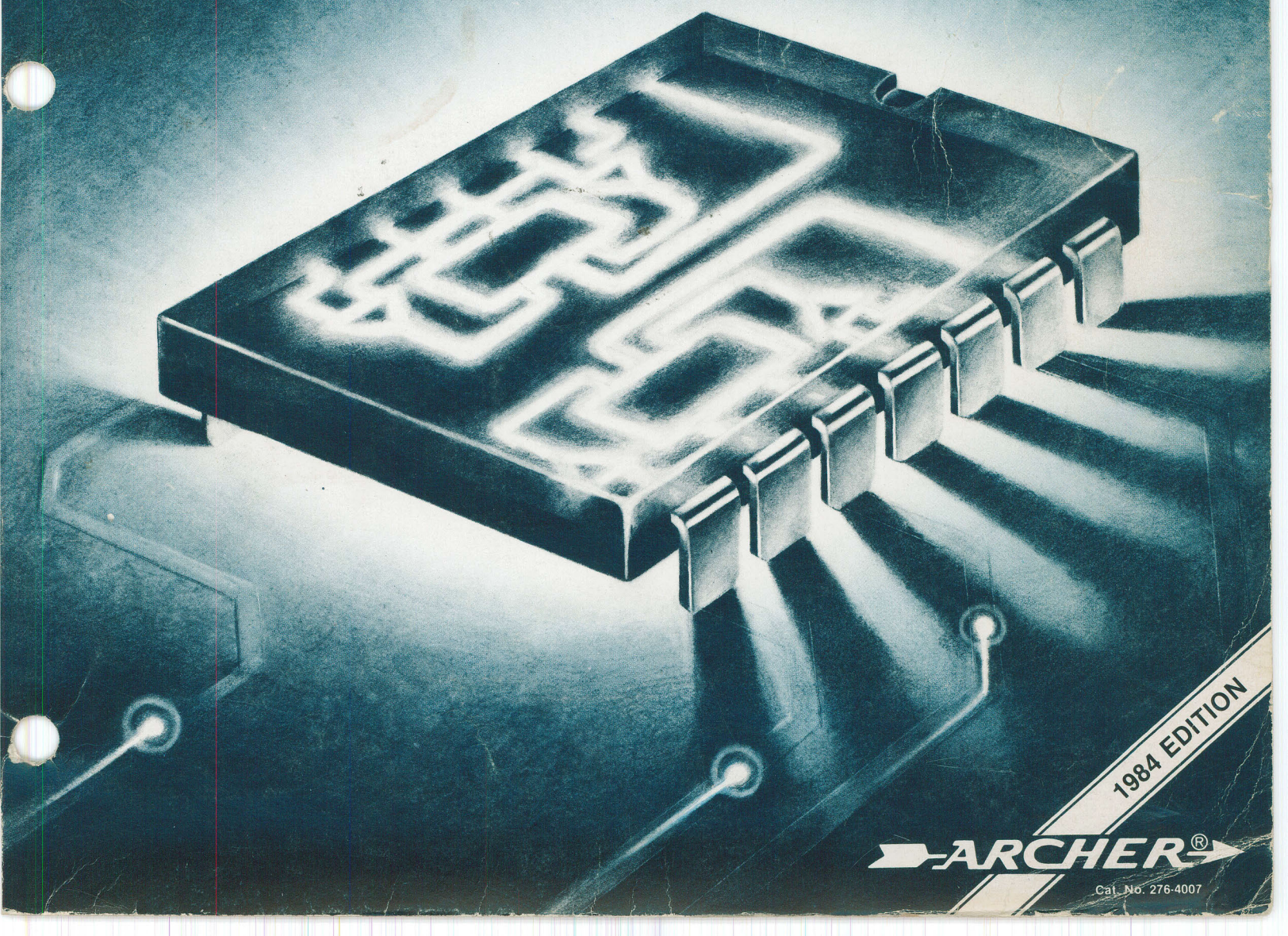
Semiconductor Reference Guide

INCLUDES OVER 100,000 SEMICONDUCTOR SUBSTITUTIONS



1984 EDITION

ARCHER®

Cat. No. 276-4007

INTEGRATED CIRCUITS BY GENERIC NUMBER

INDEX BY CATALOG NUMBER

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INTRODUCTION

This SEMICONDUCTOR REFERENCE HANDBOOK is intended to be just that—a reference handbook. It is not a definitive text book on semiconductors. It is a compilation of data on Radio Shack's line of prime-quality ARCHER semiconductors. Every ARCHER device covered in this Handbook is guaranteed prime—they are not "fall-outs" or "seconds"; all are top-quality, with known JEDEC, EIA or manufacturer's numbers.

At the back of the book is a cross-reference listing for replacement of Transistors, Diodes and other interchangeable semiconductor devices. The total number of cross-referenced devices exceeds 100,000. These cross-reference/replacement listings are computer-selected and are based on careful analysis of important parameters of the listed devices.

NOTE: If you can't find a replacement listing for a device you require, refer to the specification listings of the appropriate ARCHER family device. Often you will be able to make suitable replacements based on the information presented.

Each ARCHER replacement should meet or exceed the required parameters. However, due to differences in Quality Control and Manufacturing procedures (which often allow for or result in broad parameter variations), and because many of the ARCHER devices are capable of better performance than the original, Radio Shack does not guarantee, nor does it imply, that the listed items will provide an exact replacement in **every** instance. Therefore we recommend that you check the voltage and current requirements of the circuit (and other pertinent specifications) before replacement and compare with the specifications listed for that particular ARCHER device.

HOW TO USE THIS BOOK

This book has been prepared to aid in BOTH replacement and original applications of Semiconductor devices. The information included will be invaluable for the service technician as well as the circuit designer (whether he be an engineer, hobbyist, student or electronics experimeter).

We have included hints on handling Semiconductor devices, operating considerations, and some simple tests to aid you in evaluating the quality of the device in existing equipment (and thus the need for replacement). Also, a complete section on the specifications for each of the ARCHER devices is included; if there is any question in your mind about replacement equivalents or original use, refer to the appropriate category in the book. You will find the important characteristics specified there.

The next to last section is an extensive listing of replacement and cross reference between other manufacturer's numbers (both JEDEC/EIA 2N—numbers and in-house designations) and the ARCHER devices. This listing provides for the substitution of over 82,000 semiconductors with ARCHER devices.

The final section includes case style drawings and some handy reference notes, a comprehensive glossary of commonly used words, plus symbols and abbreviations.

CARE AND HANDLING OF TRANSISTORS

Most modern transistors are somewhat immune from mechanical shock; however, it is always a good idea to keep them from excessive mechanical shocks, especially the metal-case type (avoid dropping, etc).

When cutting transistor leads, use scissor-type cutting tools (rather than diagonal cutting tools which use a crimping action). Crimp-type cutting tools produce a mechanical shock along the lead which when transmitted to the semiconductor chip or material can cause fracture. Consider the force with which the cut lead flies off the crimp-type cutting tool and you have a good idea of the intensity of the equal and opposite force which acts on the lead going into the device.

It is always a good practice to use a heat-sink tool on a transistor lead when soldering (use a low-wattage iron—30-watts or less). Heat from soldering can cause problems (especially with certain types of semiconductor devices). Thus, to be sure, always use a heat-sink on the lead when soldering. Gripping the lead with long nose pliers between the solder connection and the case of the device makes a good heat-sink; or use a tool designed for such use.

SILICON OR GERMANIUM?

The quickest way to determine if a transistor is germanium or silicon type, is to check the normal emitter-base voltage drop. With NPN devices, if the base is approximately 0.25 volts positive with respect to the emitter, it is a germanium type. If the voltage is about 0.65 volts, it is a silicon type. For PNP devices, the voltage will be the same value, but opposite in polarity (0.25 volts for germanium and 0.65 for silicon).

OPERATING CONSIDERATIONS

Before replacing an original-equipment device with the recommended Archer Type:

(A) Compare the lead or terminal arrangement of the Archer replacement device with the lead or ter-

minal arrangement of the original device. If these arrangements are different, and the original transistor is a "plug in" type, bend the leads of the ARCHER device so that the base, emitter and collector leads will mate with the original transistor leads. Trim the leads after soldering in place.

CAUTION: Be particularly careful about "pin-circle" and "in-line" lead break-out type transistors. Often one manufacturer makes a type with "in-line" leads, while another may make the same type with "pin-circle" configuration. **Doublecheck both the original and the replacement device before soldering or plugging in transistors.**

BOTTOM VIEW

PIN-CIRCLE IN-LINE

(B) Certain considerations are involved whenever an original equipment transistor is replaced by one having a different type designation. When an ARCHER series transistor is used to replace an original equipment device in an untuned amplifier stage operating at a low signal level such as the untuned RF-amplifier (antenna) stage of a radio receiver, or a low-level AF amplifier stage, it is generally unnecessary to make any circuit adjustment to assure proper performance of the equipment. However, when a replacement is made in a turned RF amplifier stage, it is always advisable to check the alignment of the associated tuned circuits to assure proper tracking and to achieve the required gain without loss of stability.

(C) When replacements are made in stages operating at relatively high power levels, such as Class A and Class B AF output stages of automobile radio receivers, phonographs and AF-amplifier systems, the transistor bias should be checked and adjusted, if necessary, to protect the ARCHER replacement transistors against excessive dissipation and to minimize distortion. Means for making adjustments are generally provided in the equipment, and the necessary instructions are usually given in the equipment manufacturer's service data.

(D) When installing an ARCHER transistor as a substitute for an original equipment type in an FM tuner, TV tuner, or other circuits operating at frequencies in the VHF or UHF regions, it is extremely important not to change any of the lead lengths or position of the original circuit. Before removing the original transistor, carefully note its position with respect to other circuit components as well as the lengths and placement of the transistor leads, and duplicate these details as closely as possible with the ARCHER replacement transistor. Failure to observe this precaution can result in improper tuning or circuit instability. The same holds true for any replacement of Integrated Circuits, specially in FM radios and TV Receivers. Failure to observe this precaution can result in damage in the device. Transistor substitution in tuned circuits will often require realignment of the circuit.

SILICON VS SELENIUM RECTIFIERS

Silicon rectifiers are inherently more efficient than selenium or other metallic-oxide type rectifiers. When a silicon rectifier is used to replace a selenium rectifier in the power supply of a typical line-operated radio or TV receiver, the silicon rectifier will frequently deliver higher DC output voltage than the original device.

In some cases, this higher supply voltage may improve the performance of the equipment. However, in many other cases, it may immediately or eventually damage filter capacitors and/or other components which were designed to withstand only the voltage delivered by the original selenium rectifier. To prevent such damage, it is generally advisable to insert a power type resistor in series with the silicon rectifier either on the input side, between the AC supply and the rectifier, or on the output side between the rectifier and the first filter capacitor. The value of this resistor will depend on the required reduction in the DC output voltage and on the DC load current of the equipment. This value may be determined experimentally or calculated from the equation:

$$R = \frac{E}{I}$$

where R is the required resistance in ohms, E the required reduction in DC output voltage in volts and I the DC load current in amperes.

The wattage rating of the resistor should be at least 2 X EI (in no case less than 10 watts).

SOLDERING PRECAUTIONS

Extreme care should always be used in making solder connections to semiconductors. Momentary application of excessive heat, or even prolonged application of a properly heated soldering tool to a semiconductor lead or terminal, can permanently damage the device. Observe the following precautions in soldering a semiconductor lead or terminal:

1. Solder as far as possible from the body of the semiconductor.
2. Never, apply heat or molten solder to a lead or terminal for longer than 10 seconds or at a point closer than 1/16 inch to the body of the device.
3. Use a low voltage iron (30 watts or less) specifically intended for use with transistors or miniature circuit components.
4. Keep the surfaces to be soldered clean and the tip of the soldering tool adequately tinned so that the connection can be made as quickly as possible.
5. Always use a heat sink on the lead when soldering. Gripping the lead or terminal with longnose pliers between the solder connection and case or body allows the pliers to act as a heat sink, conducting heat away from the internal elements of the device.

ABOUT CASE DIMENSIONS

In some instances, the case of an ARCHER Semi-

conductor may be slightly taller or thicker than that of the original device or have a slightly different shape, particularly if the original device is a foreign type not made to U.S.A. EIA (JEDEC) standards. These mechanical differences should not affect the performance of the equipment in which the replacement is made and normally will not prevent or complicate the installation of the ARCHER replacement device.

You should realize that cross-reference substitution listings are created based **on electrical parameters (not necessarily on mechanical size or type).** Thus, when you make substitutions based on our listings, check for physical/mechanical compatibility. If space is limited, it would be a good idea to check physical dimensions as well as electrical specs before making substitution.

GENERAL PRECAUTIONS

ARCHER transistor and ARCHER semiconductors should not be inserted or withdrawn from circuits with the power on, because transient currents may cause permanent damage to the device. In some cases ARCHER semiconductors are in metal cans and thus could possibly become shock hazards if they are allowed to operate at a voltage appreciably above or below ground potential.

For the most effective protection, a power transistor should be operated with an adequate heat sink and with the lowest value of resistance or impedance in the emitter-to-base circuit consistent with driving signal considerations. The transistor should be protected against extremely high collector voltage pulses which may be generated when the device is operated with inductive loads particularly when current transients are present.

When replacing a power transistor or rectifier which is attached to the equipment chassis, or to a special heat sink, observe the following precautions:

A. In the case of oxide coated metal washers or wafers, which are frequently used as electrical insulators between the cases of power transistors and the chassis or heat sink, it is important not to scratch, chip or otherwise damage the oxide surface.

B. When installing an ARCHER power transistor, where a mica or oxide coated metal washer was used to insulate the case of the original device electrically from the case, apply a thin coating of Heat Sink Compound (Radio Shack Number 276-1372) between the washer and the chassis or heat sink.

TESTING A TRANSISTOR

Before replacing a transistor you want to be sure it needs to be replaced. Always check the entire circuitry to be sure the transistor requires replacement.

The best method for checking transistors is to use a good transistor checker (dynamic in-circuit and out-of-circuit type). However, a sensitive VOM can give you a good indication of the quality of the device.

I. In-Circuit Testing

A. First, check to see if the emitter-base junction is forward-biased. An NPN transistor should show the base 0.2 to 0.65 volts positive with respect to the emitter (approximately 0.25 volts for a germanium type and 0.6 volts for silicon). A PNP transistor should show the base 0.2 to 0.65 volts negative with respect to the emitter (0.25 volts for germanium and 0.6 volts for silicon).

B. Check to see if the device is functioning as an amplifier. Short the emitter-base junction to remove forward bias. Voltage at the collector lead should rise to approximately the potential of the collector supply buss line. Any difference is caused by I_{CES} (collector-to-base leakage current). The closer the collector voltage approaches the buss line, the lower I_{CES} is and the better the transistor.

II. Out-of-Circuit Testing

Again, for the best indication of transistor quality, use a good transistor checker. However, an ohmmeter can be used as described here.

Before using the ohmmeter, find out which polarity of the internal ohmmeter battery is connected to which test lead (not all ohmmeters have the + battery polarity connected to the red lead and the − battery polarity connected to the black lead). To determine the polarity of the leads when using the ohmmeter function, use an external voltmeter or study the schematic of your VOM.

Also, remember that in most transistor circuits you are dealing with low voltages and currents (in some cases, very low). Therefore, **NEVER** use RX1 scale (extensive currents can flow through a junction, permanently damaging the transistor). It is best to determine the maximum amount of current available in each resistance range before using an ohmmeter for testing semiconductor junctions.

After you have evaluated your VOM for the above and are sure you will not damage a transistor (with excessive current or voltage in any given ohmmeter range), proceed as follows:

A. Small Signal PNP Germanium Transistors
   1. Connect the positive lead of your ohmmeter to the emitter. Connect the negative lead to the base. You should read 200-500 ohms.
   2. Connect the negative lead to the collector. You should read 10K-100K. Shorting collector base, the resistance should decrease.

B. Small Signal NPN Germanium Transistors
   Reverse the polarity of the leads; the readings should be approximately the same.

C. Power PNP Germanium Transistors
   1. Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 35-50 ohms.
   2. Connect the negative lead to the collector The reading should be several hundred ohms. Shorting collector to base, the resistance should decrease.

D. Power NPN Germanium Transistors
   Reverse the polarity of the leads; the reading should be approximately the same.

E. Small Signal PNP Silicon Transistors
   1. Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 1K-3K.
   2. Connect the negative lead to the collector. The reading should be very high (may show as an "open").

F. Small Signal NPN Silicon Transistors
   Reverse the polarity of the leads; the readings should be approximately the same.

G. Power PNP Silicon Transistors
   1. Connect the positive lead to the emitter. Connect the negative lead to the base. The reading should be 200-1K.
   2. Connect the negative lead to the collector. The reading should be about 1 megohm or more.

H. Power NPN Silicon Transistors
   Reverse the polarity of the leads; the readings should be approximately the same.

The resistance readings noted above can only be approximate; as long as you obtain somewhat **proportionate** readings (emitter-base readings as compared to emitter-collector), you can safely assume the transistor is OK.

HANDLING OF INTEGRATED CIRCUITS

Because MOS devices have extremely high input resistance, they are susceptible to damage when exposed to static electrical charges (even electrical charges that normally build up on the human body can cause damage). To avoid possible damage to the devices during handling, testing, or actual operation, the following procedures should be observed:

1. Except when being tested or in actual operation, the leads of devices should be in contact with a conductive material, to avoid build-up of static charge.
2. Soldering iron tips, tools, metal parts of fixtures and handling facilities should be grounded.
3. Transient voltages may cause permanent damage to the device if it is removed or inserted with the power on.
4. Do not apply signals to the input with the power supply off.
5. All unused input leads must be connected to either V_{SS} or V_{DD} (whichever is appropriate for the logic circuit involved).

DIODES AND RECTIFIERS

GENERAL PURPOSE DIODES RATINGS @ 25°C

Catalog Number	PIV (min) V	If A	Ir (max) @ Vr μA	Vf (max) @ If V	Case Style
276-1101	50	1.000	10	1.6	DO41
276-1102	200	1.000	10	1.6	DO41
276-1103	400	1.000	10	1.6	DO41
276-1104	600	1.000	10	1.6	DO41
276-1114	1000	2.500	200	1.0	A1vm
276-1122	75	0.010	250nA	1.0	A1
276-1123	60	0.085	15	1.0	A1
276-1124	5	0.010	100nA	0.340	A4
276-1141	50	3.000	500	1.2	A3q
276-1143	200	3.000	500	1.2	A3q
276-1144	400	3.000	500	1.2	A3q

ZENER DIODES—1 Watt

Catalog Number	Vz Volts ±10%	Iz @ mA	Zz @ Iz ohms max	Case Style
276-561	6.2	41	2	DO41
276-562	9.1	25	7	DO41
276-563	12.0	21	9	DO41
276-564	15.0	17	14	DO41
276-565	5.1	49	7	DO41

BRIDGE RECTIFIERS

Catalog Number	PIV (min) V	If (max) A	Case Style
276-1146	50	4	M532a
276-1151	50	1.4	M548
276-1152	100	1.4	M548
276-1161	50	1	Y1
276-1171	100	4	M532a
276-1173	400	4	M532a
276-1180	50	6	M532a
276-1185	50	25	—

BIPOLAR TRANSISTORS

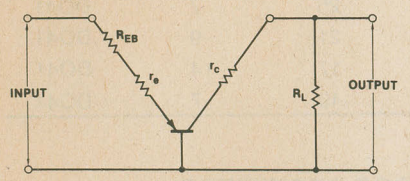
Catalog Number	Direct Commercial Equivalent	Mat.	Appli.	Polarity	Power Diss. @25°C Free Air	f_T Typical MHz	V_{CBO} V	V_{CEO} V	V_{EBO} V	I_C Max	I_B Max	h_{FE}	@V_{CE} V	@I_C mA	I_{CBO} at max V_{CB}	Case Style
276-2007	2N1305	G	S.	PNP	150mW	5	30	—	25	300mA	—	40	1	10	6μA	TO5
276-2009	MPS2222A	S	G.P.	NPN	500mW	300	75	40	6	800mA	—	50	10	1	10nA	TO92
276-2010	PN2484	S	LL	NPN	360mW	15	60	60	6	50mA	—	250	5	1	10nA	TO92
276-2016	MPS3904	S	S	NPN	350mW	300	60	40	6	200mA	—	100	10	1	50nA	TO92
276-2017	TIP31	S	P	NPN	40W‡	3	40	40	5	3A	1A	10-50	4	3A	300μA	TO220AB-2
276-2020	TIP3055	S	P	NPN	90W‡	3	100	70	7	15A	7A	20	4	4A	1mA	TO220
276-2023	MPS2907	S	S	PNP	400mW	200	60	40	5	600mA	—	50	10	1	20nA	TO92
276-2027	MJE34	S	P	PNP	90W‡	3	40	40	5	10A	3A	20-100	4	3A	220μA	TO220
276-2030	2N3053	S	P	NPN	1W	100	60	40	5	700mA	—	50	10	150	—	TO5
276-2032	MPS3638	S	RF/IF	PNP	350mW	100	25	25	4	500mA	—	30	3	10	10nA	TO92
276-2041	2N3055	S	P	NPN	115W‡	2.5	100	60	7	15A	7A	50	4	1A	—	TO3
276-2043	MJ2955	S	P	PNP	150W‡	4	100	60	7	15A	7A	70	10	0.5	—	TO3
276-2044	MRF901	S	UHF	NPN	300mW	2500	25	15	2	30mA	—	80	5	5	50nA	MACRO-X
276-2048	2SD313	S	P	NPN	30W‡	8	60	60	5	3A	—	40-320	2	1	100μA	TO220
276-2051	2SC945	S	G.P.	NPN	250mW	250	60	50	5	100mA	—	60-600	6	1	100nA	TO92J
276-2055	2SC1308	S	SW	NPN	50W‡	—	1400	400	6	7A	0.8A	3	2	4A	5mA	TO3
276-2057	2N4124	S	G.P.	NPN	350mW	300	30	25	5	200mA	—	480	10	2	0.1μA	TO92
276-2058	2N4401	S	G.P.	NPN	350mW	250 min.	40	60	6	600mA	—	500	10	1	0.1μA	TO92
276-2059	MPSA06	S	P	NPN	625mW	100	80	80	4	500mA	—	50 min.	1	100	0.1μA	TO92
276-2060	MPSA13	S	P*	NPN	625mW	2	30	30	10	500mA	—	10,000	5	100	100nA	TO92
276-2061	MPSA42	S	G.P.	NPN	625mW	50	300	300	6	500mA	—	40 min.	10	30	0.1μA	TO92
276-2068	TIP120	S	P	NPN	65W‡	0.1	60	60	5	5A	120mA	2500	3	500	0.2mA	TO220AB-2

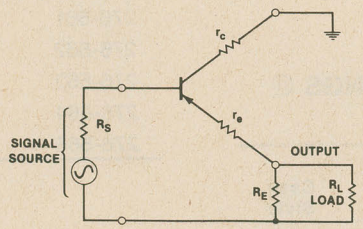
NOTE: All ratings given are for 25°C except where otherwise noted. ‡With heat sink.

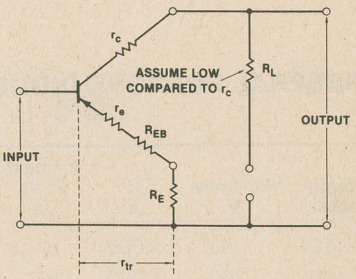
MATERIAL:
S—Silicon; G—Germanium

APPLICATION:
S—Switch
G.P.—General purpose
P—Power amp/switch
RF/IF—RF/IF frequency
*—High Gain Darlington
UHF—Ultrahigh frequency
LL—Low Level
SW—TV Sweep

USEFUL INFORMATION







Parameters of Common-Base Circuit

Input Impedance $Z_{in} = r_{tr}$

Load Impedance $Z_L = R_L$ in parallel with input impedance of following stage.

Current Gain $A_i = \alpha = \frac{\beta}{1+\beta}$
(In practice, α is 0.95 to 0.995, or approximately 1.)

Voltage Gain $A_v \approx \frac{Z_L}{r_{tr}} = g_m Z_L$

Parameters of Common-Collector Circuit

Input Impedance $Z_{in} = (\beta + 1)Z_L$
where,
Z_L is R_L in parallel with R_E.

Output Impedance $Z_{out} = \frac{R_S}{\beta+1}$
where,
R_S is the output impedance of the signal source.

Current Amplification $A_i \approx \beta$

Voltage Amplification A_v = Less than unity

Parameters of Common-Emitter Circuit

Input Impedance $Z_{in} = h_{fe} r_{tr}$

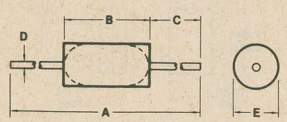
Load Impedance $Z_L = R_L$ in parallel with input impedance of next stage.

Current Gain $A_i = \frac{\Delta I_C}{\Delta I_B} = h_{fe}$
where,
$h_{fe} = \beta = \frac{I_c}{I_b} = \frac{\alpha}{1-\alpha}$

Voltage Gain $A_v = \frac{\Delta V_C}{\Delta V_B} = \frac{Z_L}{r_{tr}} = g_m Z_L$

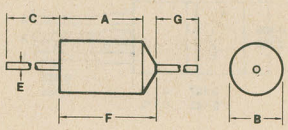
Power Gain $A_p = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \beta \frac{Z_L}{r_{tr}}$

A1



May show color bands to denote polarity.

A3



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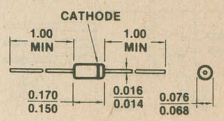
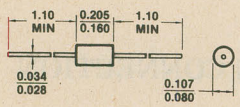
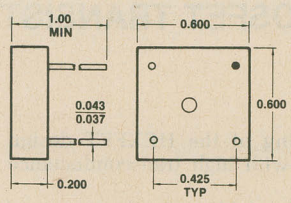


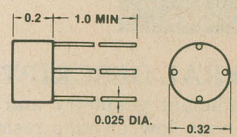
DO41



M532A

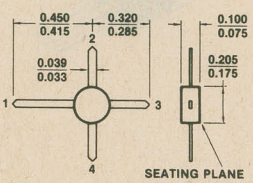


M548



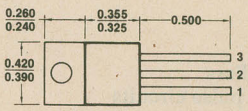
Positive: Red or Square Lead

MACRO-X



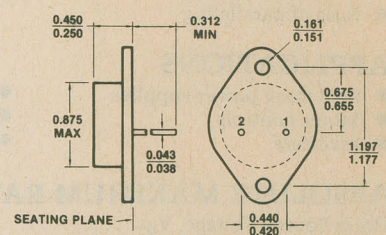
1-COLLECTOR
2-EMITTER
3-BASE
4-EMITTER

MU27



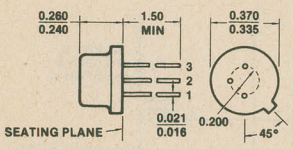
SCR	TRIAC
1-CATHODE	1-ANODE 1
2-ANODE	2-ANODE 2
3-GATE	3-GATE

TO3



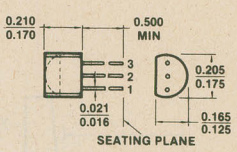
1-BASE
2-EMITTER
CASE-COLLECTOR

TO5



1-EMITTER
2-BASE
3-COLLECTOR

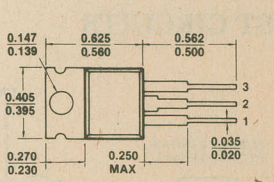
TO92



N-CHANNEL FET	UNIJUNCTION	BIPOLAR	BIPOLAR J*
1-SOURCE	1-BASE 1	1-EMITTER	1-EMITTER
2-GATE	2-EMITTER	2-BASE	2-COLLECTOR
3-DRAIN	3-BASE 2	3-COLLECTOR	3-BASE

*Japanese device types

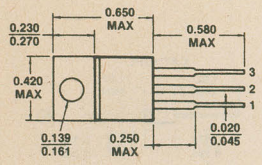
TO220



BIPOLAR	TRIAC
1-BASE	1-ANODE 1
2-COLLECTOR	2-ANODE 2
3-EMITTER	3-GATE

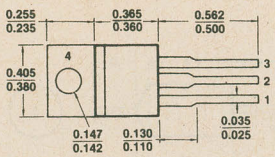
QUICK CASE REFERENCE

TO220AB



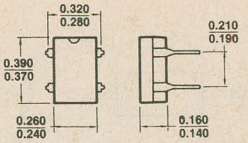
1-GATE
2-DRAIN
3-SOURCE

TO220AB-2



1-BASE
2-COLLECTOR
3-EMITTER
4-COLLECTOR

Y1



SPECIAL TRANSISTOR (N-CHANNEL MOSFET)

IRF511
276-2072

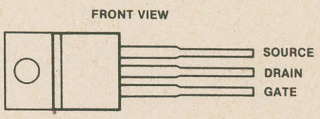
N-CHANNEL MOSFET TRANSISTOR

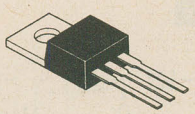
GENERAL DESCRIPTION

The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

This transistor also features all of the well established advantages of MOSFETs such as voltage control, freedom from second breakdown, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

PIN CONNECTION





FEATURES

- Fast switching
- Low drive current
- Ease of paralleling
- No second breakdown
- Excellent temperature stability

APPLICATIONS

- Switching power supplies
- Motor controls
- Inverters
- Choppers
- Audio amplifiers
- High energy pulse circuits

ABSOLUTE MAXIMUM RATINGS

Drain-Source Voltage, V_{DS} 60V
Drain-Gate Voltage (R_{GS} = 1 MΩ), V_{DGR} 60V
Gate-Source Voltage, V_{GS} ..... ±20V
Continuous Drain Current, I_D @ $T_C \cong 86°C$ 3A
Pulsed Drain Current, I_{DM} 8A
Maximum Power Dissipation, P_D 20W
Linear Derating Factor 0.16W/K
Inductive Current, Clamped, I_{LM} (See Fig. 1) L = 100 μH 8A
Operating Temperature Range, T_J ..... −55 to +150°C
Storage Temperature Range, T_{stg} ..... −55 to +150°C

TEST CIRCUITS

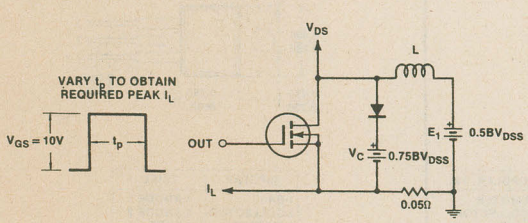


Figure 1—Clamped Inductive Test Circuit and Waveform

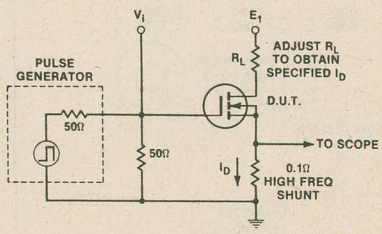
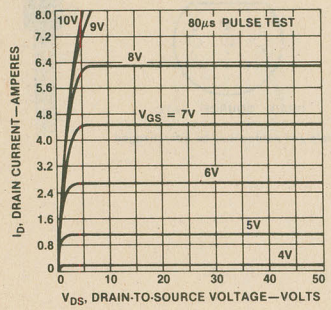


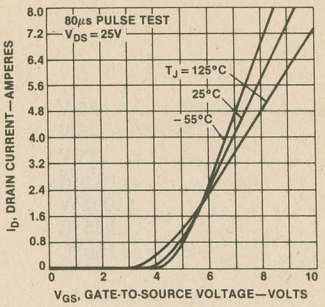
Figure 2—Switching Time Test Circuit

IRF511 276-2072

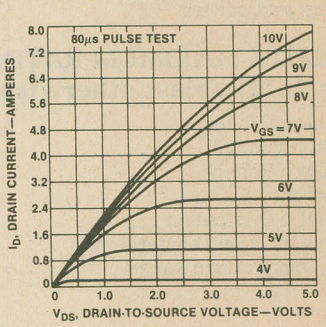
TYPICAL CHARACTERISTICS



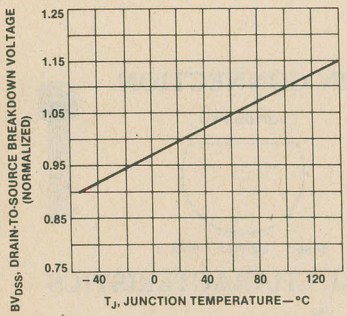
Output Characteristics



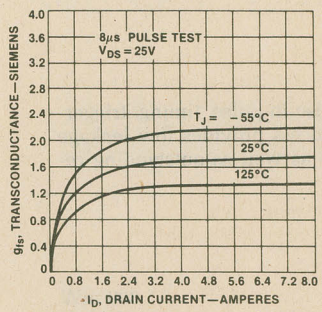
Transfer Characteristics



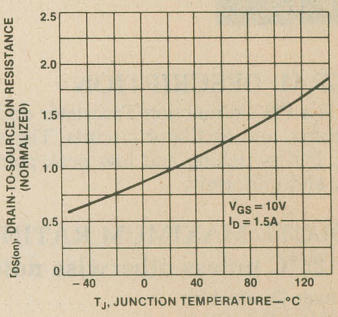
Saturation Characteristics



Breakdown Voltage vs Temperature



Transconductance vs Drain Current



Normalized On-Resistance vs Temperature

N-CHANNEL LOW POWER HEXFET

IRFD1Z3 276-2073

GENERAL DESCRIPTION

This device combines automatic insertion efficiency, a 1 watt heat sink tab with the HEXFET high performance, quality, and reliability. These space saving HEXDIPs are end-stackable in rows of any length on 100 mil centers. The low profile N-Channel HEXDIPs can be used on boards for cages with 0.5'' board spacing.

PIN CONNECTION

ABSOLUTE MAXIMUM RATINGS

Drain-to-Source Voltage, V_{DS} 60V
On-State Resistance, $R_{DS(ON)}$ 3.2Ω
Continuous Drain Current, I_D (25°C Case) 0.4A
Pulsed Drain Current, I_{DM} 1.5A
Maximum Power Dissipation, P_D 1.0W

MPF102
276-2062

SILICON N-CHANNEL JUNCTION FIELD EFFECT TRANSISTOR

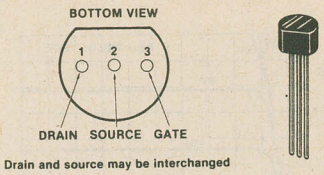
GENERAL DESCRIPTION

The MPF102 is designed for small signal applications. These include VHF amplifiers and mixers.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage	25 V
Drain-Gate Voltage	25 V
Gate-Source Voltage	25 V
Gate Current	10 mA
Total Device Dissipation	310 mW
Operating Junction Temperature	125°C
Storage Temperature Range	−65 to +150°C

PIN CONNECTION



Drain and source may be interchanged

MU4891
276-2029

PN UNIJUNCTION TRANSISTOR

GENERAL DESCRIPTION

This is a PN Unijunction Transistor designed for use in pulse, timing, triggering, sensing, and oscillator circuits. The annular process provides low leakage current, fast switching and low peak-point currents as well as outstanding reliability and uniformity.

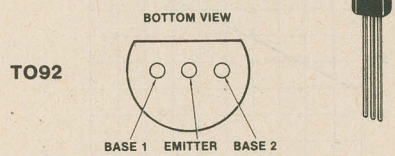
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

RMS Power Dissipation	300 mW
RMS Emitter Current	50 mA
Peak Pulse Emitter Current	1.0 Amp
Emitter Reverse Voltage	30 Volts
Intrinsic Standoff Ratio (η) (V_{B2B1} = 10V) Note 1	0.82 η
Interbase Resistance (r_{BB}) (V_{B2B1} = 3.0 V, I_E = 0)	9.1 k ohms
Interbase Resistance Temperature Coefficient ($\propto Ir_{BB}$) (V_{B2B1} = 3.0 V, I_E = 0, T_A = −65°C to 100°C)	0.9%/°C
Emitter Saturation Voltage ($V_{EB1(sat)}$) (V_{B2B1} = 10 V, I_E = 50 mA) Note 2	4.0 Volts
Modulated Interbase Current ($I_{B2(mod)}$) (V_{B2B1} = 10 V, I_E = 50 mA)	15 mA
Emitter Reverse Current (I_{EB20}) (V_{B2E} = 30 V, I_{B1} = 0)	10 nA
Peak Point Emitter Current (Ip) (V_{B2B1} = 25 V,)	5.0 μA
Valley Point Current I_V) (V_{B2B1} = 20 V, R_{B2} = 100 ohms) Note 2	4.0 mA
Base-one Peak Pulse Voltage (V_{0B1}) (Note 3, Figure 2)	5.0 Volts
Storage Temperature Range	−65 to +150°C

NOTES

1. Intrinsic standoff ratio.
   η, is defined by equation:
   $$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$
   Where V_P = Peak Point Emitter Voltage
   V_{B2B1} = Interbase Voltage
   $V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop (≈0.5V @ 10μA)
2. Use pulse techniques: PW≈300 μs duty cycle ≤2% to avoid internal heating due to interbase modulation which may result in erroneous readings.
3. Base-One Peak Pulse Voltage is measured in circuit of Figure 2. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

PIN CONNECTION



TYPICAL CHARACTERISTICS

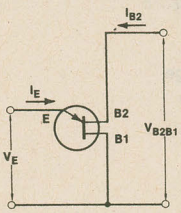


Figure 1—Unijunction Transistor Symbol and Nomenclature

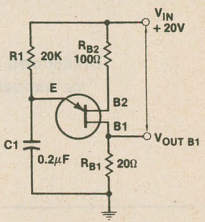
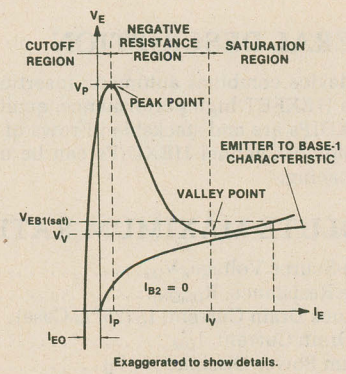


Figure 2—Typical Relaxation Oscillator



Exaggerated to show details.

Figure 3—Static Emitter Characteristic Curves

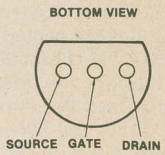
SILICON N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

2N3819
276-2035

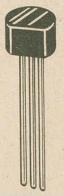
GENERAL DESCRIPTION

The 2N3819 is designed for general purpose small-signal applications. It features low capacitance between drain and gate terminals and an excellent high-frequency figure of merit. It achieves a low noise figure and good power gain with low crossmodulation and intermodulation.

PIN CONNECTION



T092

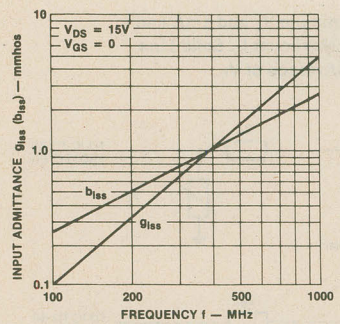


ABSOLUTE MAXIMUM RATING
(T_A = 25°C unless otherwise noted)

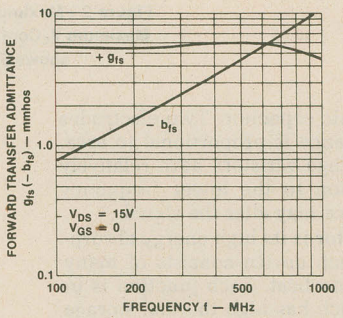
Gate-Source Breakdown Voltage BV_{GSS} . . . . . −40 V
Zero Gate Voltage Drain Current I_{DSS} . . . . . 20 mA
Forward Transconductance g_{fs} . . . . . 7.0− mmhos
Reverse Gate Leakage I_{GSS} . . . . . −100 pA
"ON" Resistance r_{DS} . . . . . 500 ohms
Pinch Off Voltage $V_{GS(OFF)}$ . . . . . −6.0 V
Output Conductance g_{os} . . . . . 10 μmhos
Feedback Capacitance C_{rss} . . . . . 0.9 pF
Input Capacitance C_{iss} . . . . . 4.0 pF
Power Gain G_{PS} . . . . . 12 dB
Power Dissipation . . . . . 360 mW

TYPICAL CHARACTERISTICS

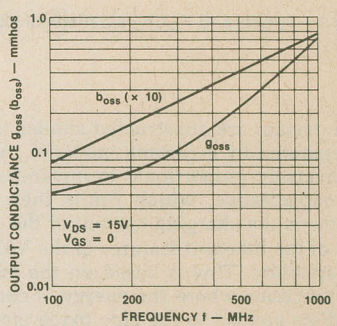
COMMON SOURCE



Input Admittance vs Frequency

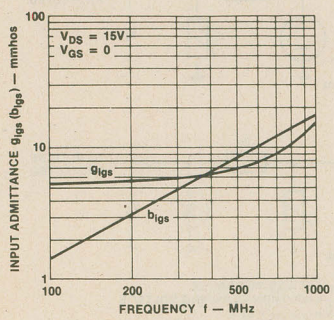


Forward Transfer Admittance vs Frequency

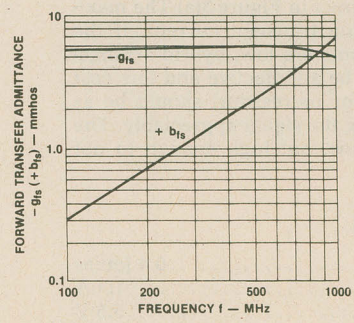


Output Conductance vs Frequency

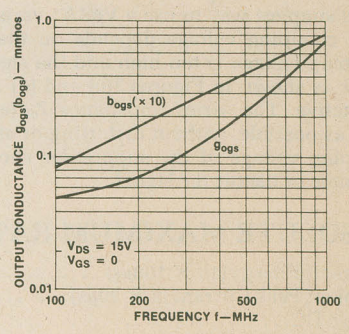
COMMON GATE



Input Admittance vs Frequency



Forward Transfer Admittance vs Frequency



Output Conductance vs Frequency

V8ZA1
276-569

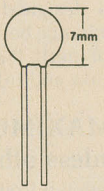
METAL DIODE VARISTOR

GENERAL DESCRIPTION

The V8ZA1 varistor is best described by a voltage current characteristic shown in Figure 1. The device is symmetrical and its V-I characteristic is quite similar to zener diodes connected back-to-back.

Figure 2 shows the V-I characteristics of the V8ZA1. The 1 mA point defines the specification limit for the minimum and maximum voltage. The maximum point is continuous into the maximum clamping voltage of the device. The thick, heavy line shows the 500-device average. In comparing the 500-device average and the maximum limits, one can see how much better the devices are than the specification indicates.

PIN CONNECTION



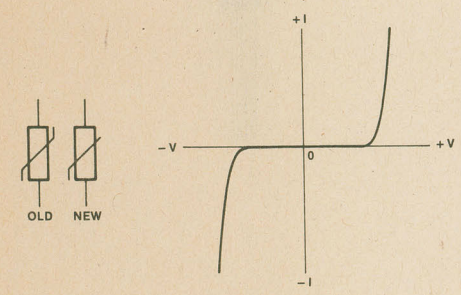


Figure 1—Symbol and V-I Characteristic of Varistors

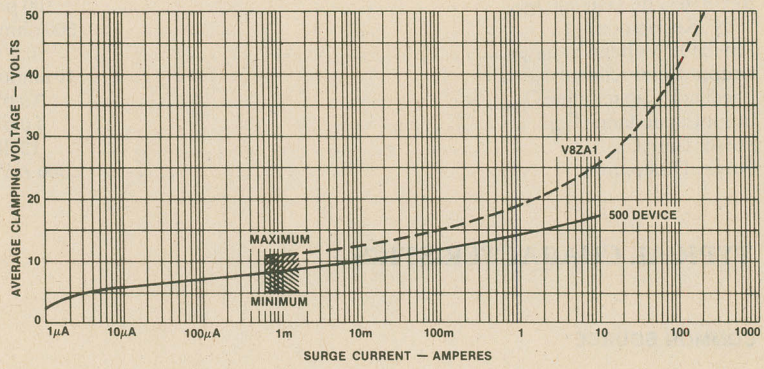


Figure 2—Maximum and Minimum V_C and 1mA and Maximum V_CContinuous to Maximum I_C. Solid Line shows 500 DeviceAverage of V_C

The devices are constructed similar to a ceramic capacitor. Two electrodes are separated by a ceramic material. As capacitance is proportional to area, and inversely proportional to thickness, low-voltage varistors have relatively high capacitance, which limits their application to the lower frequency domain, as the charging current of the capacitance may alter the signal.

One of the inherent features of the V8ZA1 varistor is its high energy absorption capability. This is based on the fact that each device consists of many small junctions where the energy is converted into heat. Each junction is in immediate contact to the zinc oxide material which has high thermal storage capability and yields a device having low peak temperatures, which makes it extremely reliable with superior overload capability.

The new low-voltage varistors can be used to protect low-voltage circuits of 5V and lower: all integrated circuits, systems containing low-voltage IC's, memories, test equipment, data processing equipment using large, mini, or micro-computers, input-output circuits, sensing circuits, current loops, sensing and interlocking circuits.

The simplest way to use a V8ZA1 varistor is shown in Figure 3(a) The maximum clamping voltage depends on the maximum transient current. If the clamping voltage is too high and the signal currents are low, hybrid arrangements as shown in Figures 3(b) and (d) may still be an effective and low cost alternative. The series impedance Z_S (an inductor or resistor) should be as large as possible, without distorting or attenuating the signal appreciably. The clamping voltage of the suppressor should be low, but high enough to not attenuate or distort the signal.

ABSOLUTE MAXIMUM RATINGS

Transient Energy (10 × 100μs)	0.4 Joules
Transient Peak Current (8 × 20μs)	100A
Voltage DC	5.5 V
Voltage RMS	4 V
Voltage Clamping (8 × 20μs)	22 V
Typical Capacitance (f = 0.1-1MHz0	4500 pF
Power (Transients)	0.25 W

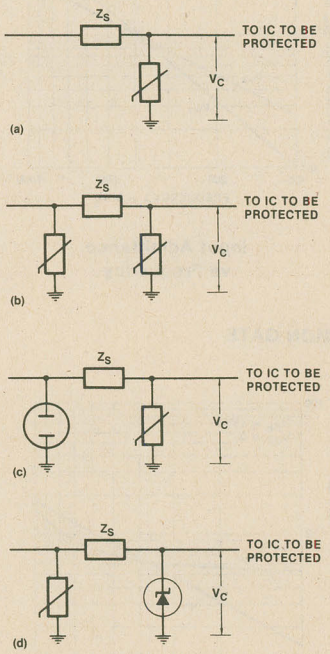
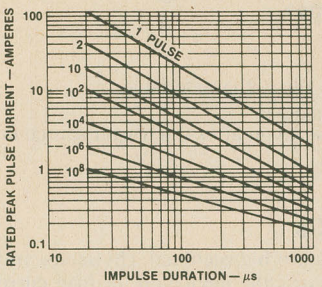


Figure 3—Possible Configurations of V8ZA1 Varistors In Combination With Other Devices

V8ZA1 276-569

TYPICAL CHARACTERISTICS



Rated Peak Pulse Current vs Impulse Duration

APPLICATION INFORMATION

Transients exist in every ac or dc system or any wire connecting two pieces of equipment or components. The source can be lightning, high energy switching, high voltage sparkover, or fuse blowing. Every time a magnetic storage device is turned off, the energy stored in the inductance is given as:

$$E = 1/2\ L\ I^2$$

E = Energy (Joules)
L = Inductance (Henries)
I = Current (Amps)

The peak voltage is the result of collapsing the magnetic field.

$$V = -L \times \frac{di}{dt}$$

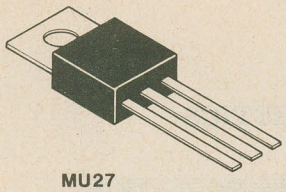
V = Induced voltage (Volts)
L = Inductance
$\frac{di}{dt}$ = Change of current

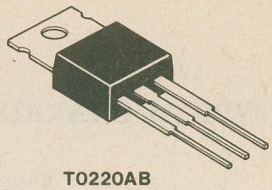
Contact arcing, capacitor discharge, and electrostatic discharge may be found any place there is energy stored in inductances, capacitors, or mechanical devices (motors and generators), and this energy is returned to a circuit. Stray capacitance and inductance may set off oscillation, making the problem even worse.

Whatever the cause of a transient, natural or man-made, the damage potential is real and cannot be causally dismissed if reliable operation of equipment is to be expected.

To properly select a transient suppressor, the frequency of occurrence, open circuit voltage, short circuit current, and source impedance must be known.

276-1000 276-1001 276-1020 276-1067 THYRISTORS


MU27


TO220AB

GENERAL DESCRIPTION

Thyristors and their trigger devices can take numerous forms, but they share these characteristics:

- They are "open circuits," capable of withstanding rated voltage until triggered.
- They become low-impedance current paths when triggered, and remain so, even after the trigger source is removed, until current through that path stops, or is reduced below a minimum "holding" level.

SCRs

Silicon-Controlled Rectifiers (SCRs) are Thyristors intended to switch load currents in one direction only, making them useful for DC and half-wave AC applications as well as full-wave applications, in which bidirectional current is routed in one direction through the SCR via a bridge rectifier.

Catalog Number	Imax A	Vmax V	I_{GT} (max) mA	V_{GT} (max) V	Case Style
276-1067	6	200	25	1.5	MU27
276-1020	6	400	25	1.5	MU27

TRIACs

Triacs are bidirectional Thyristors, in which a single trigger source turns the device on for load current in either direction. Because they do not require a bridge rectifier in order to handle full-wave AC, Triacs are useful in AC power applications that require full source power control capability to be applied to the load.

Catalog Number	Imax A	Vmax V	I_{GT} (max) mA	V_{GT} (max) V	Case Style
276-1001	6	200	50	2.5	TO220AB
276-1000	6	400	50	2.5	MU27

V130LA10A 276-570 METAL OXIDE VARISTER

GENERAL DESCRIPTION

This zinc oxide varistor is a voltage dependent symmetrical resistor which performs similarly to back-to-back zener diodes in circuit protection and offers advantages in performance and economics. When exposed to high energy voltage transients, the varistor impedance changes from a very high standby value to a very low conducting value thus clamping the transient to a protective level. The energy of the incoming high voltage pulse is absorbed by the varistor, protecting voltage sensitive components against damage.

PIN CONNECTION

FEATURES

- Excellent clamp ratio
- Fast response time (<35 nsec.)
- Low standby power drain
- No follow-on current

ABSOLUTE MAXIMUM RATINGS

Transient Energy (10 × 1000 μs) (Note 1) . . . . . 35 joules
Transient Peak Current (8 × 20 μs) (Note 2) . . . . . 4500 A
Peak Voltage @ 1 ma DC . . . . . 232 V
Peak Voltage @ 1 ma AC . . . . . 254 V
Clamping Voltage V_C @ Test Current (8 × 20 μs) . . . . . 340 V
Typical Capacitance (f = 0.1 to 1 MHz) . . . . . 1000 pF
Note 1: 10 μs rise and 1000 μs to 50% decay of peak value.
Note 2: 8 μs rise and 20 μs to 50% decay of peak value.

OPTOELECTRONIC INDEX

TRI-COLOR LIGHT EMITTING DIODE

XC-5491
276-035

GENERAL DESCRIPTION

The XC-5491 tri-state LED provides red, green, and yellow emission in the same package. This LED is a popular .200 diameter, two-leaded package containing a red and green LED chip in inverse parallel. By reversing the polarity of the applied current, the LED will emit red or green light while an AC voltage results in yellow light. The chips used in the XC-5491 are brightness matched so that the light output is uniform. This eliminates the necessity for the special drive circuits previously required with tri-state lamps.

These lamps provide the designer with the capability of efficiently displaying three functions with one indicator. This reduces the number of front panel indicators and simplifies design.

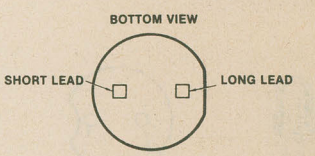
FEATURES

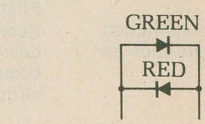
- 3 States—red, green, and yellow
- Equal brightness in all three colors
- Popular T 1¾ size package
- Wire wrappable leads

ABSOLUTE MAXIMUM RATINGS

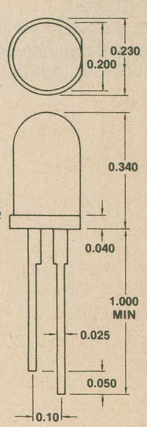
Forward Current ..... 25 mA
Peak Reverse Voltage 5V
Power Dissipation ..... 100 mW
Operating Temperature Range ..... −55 to +85°C
Lead Solder Temperature ..... 260°C

PIN CONNECTION





SHORT LEAD	LONG LEAD
Red Cathode	Red Anode
Green Anode	Green Cathode



OPTOELECTRONIC (LED)
LED INDICATORS

Catalog Number	Direct Commercial Equivalent	Peak Wave Length nM	Color	Forward Voltage V_F (V)	Reverse Voltage V_R (V)	Max DC Forward Current I_F (MA)	Max Pwr Diss P_D (MW)	Fig. No.
276-018	PR5534S	700	RED	2.5	4	100	75	5
276-019	BG5534S	555	GREEN	2.5	4	100	125	5
276-021	SLP-236B	565	YELLOW	2.8	3	30	70	6
276-022	SLP-236B	565	GREEN	2.8	3	30	70	6
276-026	—	650	RED	—	3	50	100	3
276-033	TLR-107	700	RED	2.1	4	35	100	2
276-037	SLP-235B	565	GREEN	2.8	3	30	70	5
276-041	—	700	RED	1.75	3	70	140	4
276-068	—	700	RED	1.9	—	30	—	7
276-069	—	560	GREEN	2.1	—	30	—	7
276-070	SEL-1120R	700	RED	2.5	3	30	—	1
276-073	—	—	YELLOW	2.1	—	30	—	7

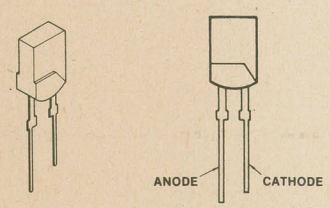


FIGURE 1
Miniature LED with diffused lens. Its features include high brightness—ideal for bar graph display—can be arranged horizontally or vertically.

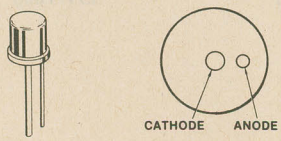


FIGURE 2
Miniature LED with diffused lens. This LED is compatible with most TTL and transistor circuits. It features a Fresnel lens design.

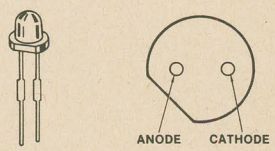


FIGURE 3
This LED features a frosted diffused lens in a plastic encapsulant. When the device is on, it appears as a large, soft light source, making it ideally suited for front panel applications.

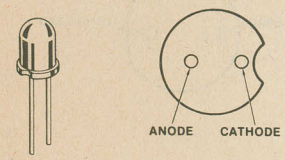


FIGURE 4
This device is a jumbo LED with a diffused lens. It can be used in applications such as pilot and indicator lamps.

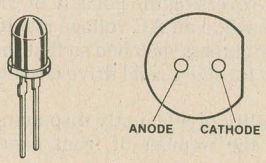


FIGURE 5
Subminiature LED with diffused lens. This device has solid state reliability and is compatible with most TTL and transistor circuits.

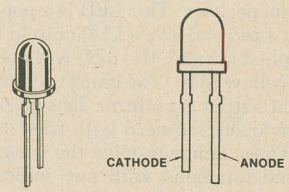


FIGURE 6
This is a frame type solid state LED with a diffused lens.

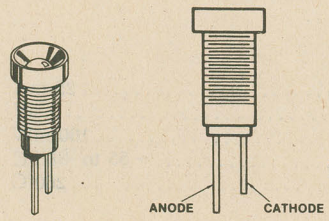


FIGURE 7
This is a subminiature LED indicator with polished chrome reflective holder.

SILICON PHOTOTRANSISTOR 276-130

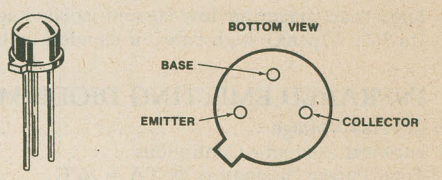
GENERAL DESCRIPTION

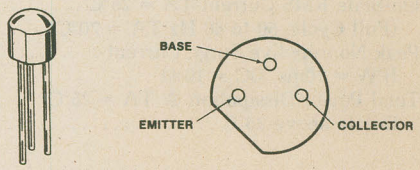
The 3 terminal phototransistor has exceptionally stable characteristics and high illumination sensitivity. The electrically connected base lead increases its applicability to various circuit designs. It features low leakage, low power requirements, TTL/DTL compatibility, a wide sensitivity range and fast response.

ABSOLUTE MAXIMUM RATINGS

Maximum Power Dissipation
Total Dissipation at 25°C Case Temperature ..... 200 mW
at 25°C Ambient Temperature ..... 100 mW
Maximum Voltages
V_{CBO} Collector to Base Voltage ..... 50 Volts
V_{CEO} Collector to Emitter Sustaining Voltage ..... 30 Volts
Maximum Current
I_C Collector Current ..... 25 mA
Maximum Temperature/Humidity
Operating Junction Temperature ..... −55 to +85°C
Storage Temperature ..... −55 to +100°C
Relative Humidity at Temperature ..... 98% to 65°C

PIN CONNECTIONS





The base lead is for testing only, it is not used in normal applications.

INFRARED PHOTOTRANSISTOR TIL414 276-145

GENERAL DESCRIPTION

The TIL414 is an NPN silicon phototransistor in A T-1 3/4 style case. It provides high speed and high photosensitivity, suitable for IR switching applications.

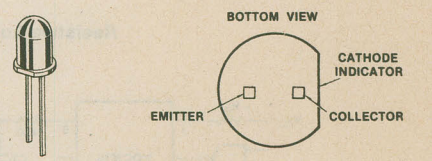
ABSOLUTE MAXIMUM RATINGS

Collector-Emitter Voltage ..... 50 V
Emitter-Collector Voltage ..... 7 V
Power Dissipation ..... 50 mW
Operating Temperature ..... −40° to +100°C

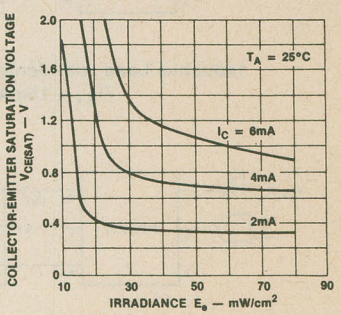
ELECTRICAL CHARACTERISTICS (Typical)

Dark Current (V_{CE} = 30 V) ..... 25 nA
Light Current (V_{CE} = 5 V●E_e = 20mW/cm²) ..... 7 mA
Collector-Emitter Saturation ..... 0.4 V
Rise Time ..... 8 μs
Fall Time ..... 6 μs

PIN CONNECTION



TYPICAL CHARACTERISTICS



Collector-Emitter Saturation Voltage vs Irradiance

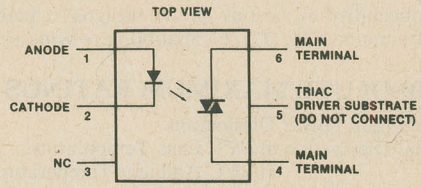
MOC3010
276-134

OPTOCOUPLER TRIAC DRIVER

GENERAL DESCRIPTION

This device consists of a gallium-arsenide infrared emitting diode, optically coupled to a silicon bilateral switch and is designed for applications requiring isolated triac triggering, low-current isolated ac switching, high electrical isolation (to 7500 V peak), high detector standoff voltage, small size, and low cost.

PIN CONNECTION



INFRARED EMITTING DIODE MAXIMUM RATINGS

Reverse Voltage ..... 3.0 volts
Forward Current—Continuous ..... 50 mA
Total Power Dissipation @ TA = 25°C ..... 100 mW

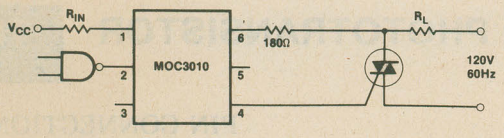
OUTPUT DRIVER MAXIMUM RATINGS

Off-State Output Terminal Voltage ..... 250 Volts
On-State RMS Current TA = 25°C ..... 100 mA
(Full Cycle, 50 to 60 Hz TA = 70°C) ..... 50 mA
Peak Nonrepetive Surge Current ..... 1.2 A
(PW = 10ms, DC = 10%)
Total Power Dissipation @ TA = 25°C ..... 300 mW
Derate above 25°C ..... 4.0 mW/°C

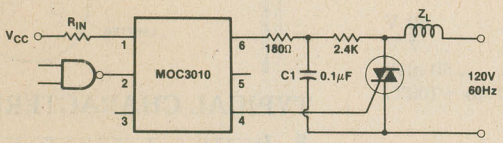
TOTAL DEVICE MAXIMUM RATINGS

Isolation Surge Voltage (1s) ..... 7500 Vac
(Peak ac Voltage, 60 Hz. 5 Second Duration)
Total Power Dissipation ..... 330 mW
Junction Temperature Range ..... −40 to +100°C
Ambient Operating Temperature Range ..... −40 to +70°C
Storage Temperature Range ..... −40 to +150°C
Soldering Temperature (10s) ..... 260°C

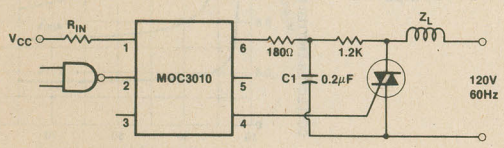
APPLICATIONS



Resistive Load

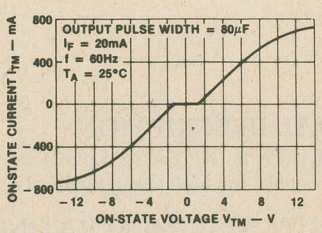


Inductive Load with Sensitive Gate Triac
($I_{GT} \leq 15mA$)

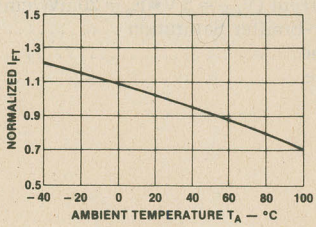


Inductive Load with Non-Sensitive Gate Triac
($15mA < I_{GT} < 50mA$)

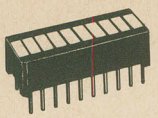
TYPICAL CHARACTERISTICS



On-State Current vs On-State Voltage



Trigger Current vs Temperature



HIGH EFFICIENCY RED BAR GRAPH DISPLAY

MV57164
276-081

GENERAL DESCRIPTION

The MV57164 is a 10 segment bar graph display with separate anodes and cathodes for each light segment. The packages are end stackable.

FEATURES

- Large segments, closely spaced
- End stackable
- Fast switching, excellent for multiplexing
- Low power consumption
- Directly compatible with IC's
- Wide viewing angle
- Standard .3″ DIP leading spacing

ABSOLUTE MAXIMUM RATINGS
(25°C Free Air Temperature Unless Otherwise Specified)

Power dissipation 750mW
Continuous forward current
  Total ..... 300 mA
  Per segment ..... 30 mA
Reverse voltage
  Per segment ..... 6.0 V
Storage and operating temperature ..... −40 to +85°C
Solder time 5 sec. ..... 260°C

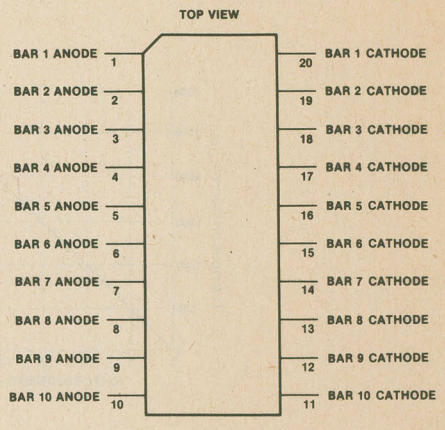
TYPICAL THERMAL CHARACTERISTICS

Thermal resistance junction to free air Φ JA ..... 160° C/W
Wavelength temperature coefficient (case temp) ..... 1.0 A/°C
Forward voltage temperature coefficient ..... −2.0 mV/°C

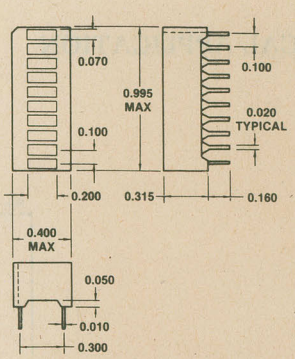
ELECTRO-OPTICAL CHARACTERISTICS

Forward Voltage ..... 2.5 V
Peak emission wavelength 630nm
Spectral line half width 40nm
Dynamic resistance
Segment ..... 26 ohms
Capacitance ..... 35 pF
Switching Time ..... 400 ns
Reverse Voltage ..... 6.0 V

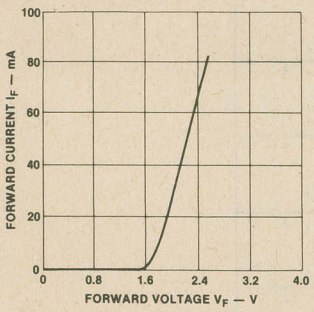
PIN CONNECTION



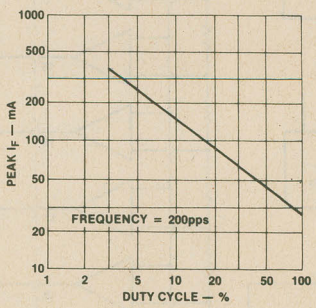
DIMENSIONAL DIAGRAM



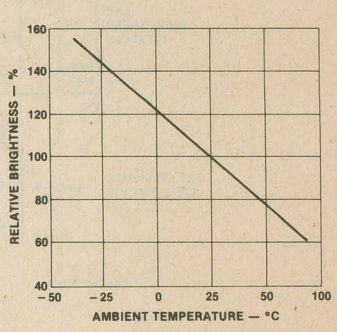
TYPICAL CHARACTERISTICS



Forward Current vs Forward Voltage



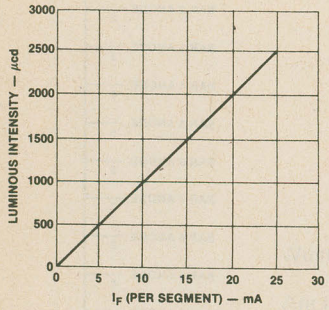
Luminous Intensity vs Forward Current



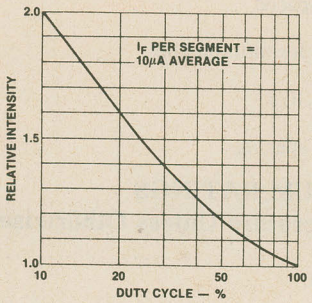
Luminous Intensity vs Ambient Temperature

MV57164 276-081

TYPICAL CHARACTERISTICS (Cont'd)



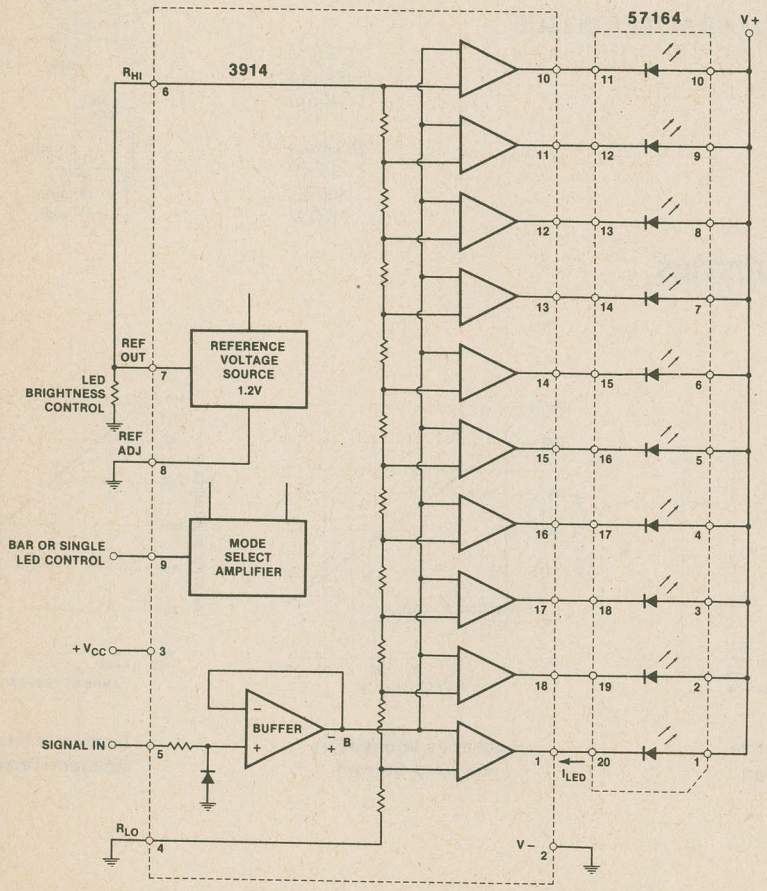
Maximum Peak Current vs Duty Cycle

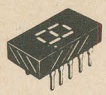


Luminous Intensity vs Duty Cycle

TYPICAL APPLICATION

Typical Drive Circuit





0.3″ SOLID STATE SEVEN SEGMENT DISPLAY 276-053

GENERAL DESCRIPTION

The 276-053 is a common anode LED numeric display. The large 0.3″ high character size generates a bright, continuously uniform 7 segment display. Designed for viewing distances of up to 10 feet, this single digit display has been human engineered to provide a high contrast ratio and wide viewing angle.

FEATURES

- Fits 14 pin DIP socket
- Excellent character appearance—continuous uniform segments; wide viewing angle; high contrast
- IC compatible—1.6 V per segment
- Standard 0.3″ DIP lead configuration; PC board or standard socket mountable
- Both left and right decimal points

APPLICATIONS

- Electronic calculators
- TVs
- Radios
- Frequency counters
- Digital clocks

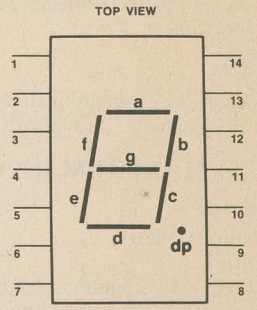
RADIANT CHARACTERISTICS (IF=20mA) T_A=25°C

Luminous Intensity..... 250 mcd
Wavelength (Peak) ..... 655 nM

ABSOLUTE MAXIMUM RATINGS

Power Dissipation T_A=25°C..... 400 mW
Average Forward Current/Segment or Decimal Pt. T_A =25°C ..... 25 mA
Peak Forward Current/Segment or Decimal Pt. T_A=12°C
(Pulse Duration 500μs) ..... 150 mA
Reverse Voltage per Segment or Decimal Pt. ..... 6 V
Operating Temperature Range ..... −20 to +85°C
Storage Temperature Range..... −20 to +85°C
Max Solder Temperature 1/16″ Below Seating Plane (t ≤ 5 sec.) ..... 230°C

PIN CONNECTION



COMMON ANODE

PIN	FUNCTION
1	CATHODE a
2	CATHODE f
3	ANODE
4	NO PIN
5	NO PIN
6	CATHODE dp
7	CATHODE e
8	CATHODE d
9	NO CONNECTION
10	CATHODE c
11	CATHODE g
12	NO PIN
13	CATHODE b
14	ANODE

ALTERNATE CONNECTION

PIN	FUNCTION
1	NO PIN
2	ANODE
3	CATHODE-f
4	CATHODE-g
5	CATHODE-e
6	CATHODE-d
7	NO PIN
8	NO PIN
9	ANODE
10	CATHODE-dp
11	CATHODE-c
12	CATHODE-b
13	CATHODE-a
14	NO PIN

CADMIUM SULPHIDE PHOTOCELL 276-116

GENERAL DESCRIPTION

A cadmium sulphide photo cell is a light variable resistor which is most sensitive in the green to yellow portion of the light spectrum. With it you can use light to control many electronic devices. Max. resistance .5 meg., min. resistance 100 ohms, max. voltage 170 V, max. wattage .2 watts, rugged epoxy case.

APPLICATIONS

- Night light
- Light control
- Burglar alarm
- Relay

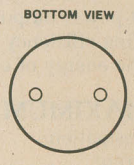
SPECIFICATIONS

- Shape..... Round
- Sensitive Area ..... .07 sq. in.
- Weight ..... 1.56 gms.
- Resistance at 1 Ftc (2870°K)..... 1.7k Ohms . 40%
- Typical Resistance 100 Ftc (2870°K)..... 100 Ohms
- Resistance Dark Minimum (1 Minute)..... 0.5 Megohms

ABSOLUTE MAXIMUM RATINGS

Max. Applied Voltage (ac or dc) ..... 170 V peak
Max. Power Dissipation at 25°C ..... 2 watts
Power Derating..... Linearly to 0 @ 75°C
Operating Temp. Range ..... −40 to +75°C

CONNECTIONS



276-142 INFRARED EMITTER AND DETECTOR

GENERAL DESCRIPTION

The 276-142 is a pair consisting of an infrared photodetector and an infrared-emitting diode. The diode is capable of emitting radiant energy in the infrared region of the spectrum.

FEATURES

- Spectrally and mechanically matched
- High power efficiency . . . typically 5 percent at 25°C

ABSOLUTE MAXIMUM RATINGS

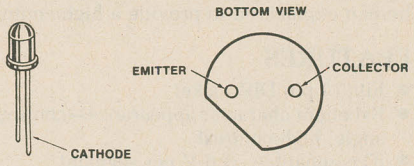
Photodetector

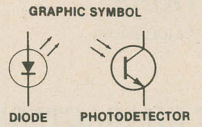
Collector-Emitter Voltage	20V
Collector Current	25mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature	50mW
Operating Free-Air Temperature Range	−40 to +80°C
Storage Temperature Range	−40 to +85°C
Lead Temperature 1/16 Inch from Case for 5 Seconds	240°C

Infrared-Emitting Diode

Reverse Voltage	2V
Continuous Forward Current	40mA
Radiant Power Output	0.5mW
Wavelength at Peak Emission	915mm

PIN CONNECTION





276-143 SUPER HIGH OUTPUT INFRARED EMITTER

GENERAL DESCRIPTION

This device is a gallium aluminum arsenide super high output infrared emitting diode. It emits non-coherent, infrared energy at 880 nm and provides significantly improved coupling efficiency to Si photo transistors and photodiodes.

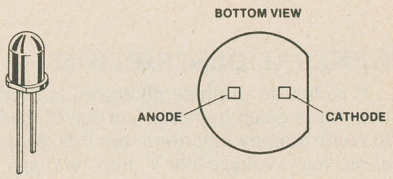
FEATURES

- GaAlAs heterostructure material. Emits at 880 nm
- Super high conversion efficiency/maximum power output
- 2× total radiant power output of 940 nm product
- Increased coupling efficiency to silicon opto devices
- Emits 3 times the energy of conventional IR emitter

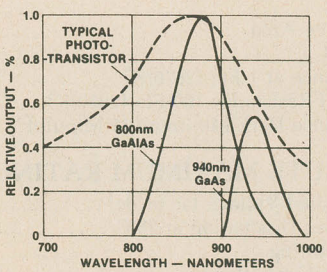
ABSOLUTE MAXIMUM RATING

Average Power Dissipation	75 mW
Average Fwd. Current	45 mA
Reverse Voltage	3.0 V
Peak Pulse Current 100μsec Duration @ 10 pps	0.30 A
Forward Voltage	1.75 V
Temp Coef of Fwd Voltage	−1.8 mV/DC
Dynamic Resistance	1.5 ohms
Angle between Half Power Intensity Points	40°
Peak Wavelength	880 nm
Line Halfwidth	80 nm
Reverse Current, Max. at 25°C	10μA
Response Time (10% to 90%)	1.5 μs
Operating, Storage, or Process Temp Range	−40 to +85°C
Solder Temp. 5 Sec 1/16 inch from case	260°C

PIN CONNECTION



SPECTRAL MATCHING COMPARISON



Relative Output vs Wavelength

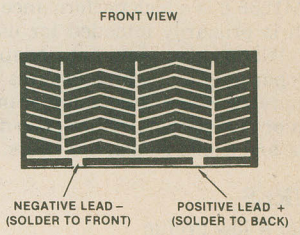
2.5×5cm SILICON SOLAR CELL 276-124

GENERAL DESCRIPTION

A solar cell is a silicon semiconductor device which converts light energy directly to electricity. A typical 2.5×5cm cell will produce 0.42 volt and up to .18 amp of usable current. The power generated is affected by the load resistance (circuit powered by cell) strength of sunlight and temperature.

Be extremely careful when soldering leads. Use only a very fine wire (#26 or thinner) and use a small soldering iron (less than 50 watts). Solar cells may be connected in series to produce more voltage and in parallel for more current.

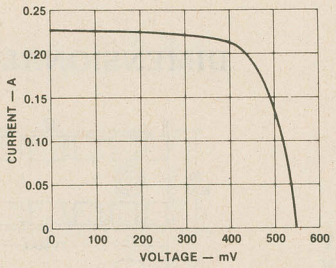
CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage (Open Circuit): 0.55V
Current (short circuit): 0.2A
(Test conditions: Full sunlight at noon on a clear day at 25°C (76°F))

TYPICAL CHARACTERISTICS

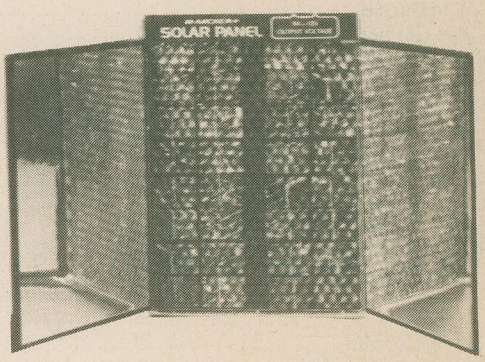


Current vs Voltage

5¾ × 4 in SILICON SOLAR PANEL 277-1250

GENERAL DESCRIPTION

This solar panel is a silicon semiconductor device which converts light energy directly into electricity. The 5¾" × 4" panel will produce a minimum of 40 mA with the switch in the 12 V position or 80 mA in the 6 V position. The power generated is affected by load resistance (circuit powered by panel), strength of sunlight and temperature.

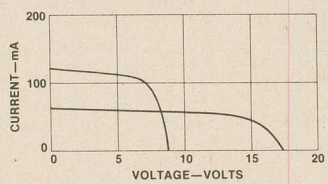


ABSOLUTE MAXIMUM RATINGS

6V Mode
No Load Voltage (Open Circuit) ..... 8.6 V
No Load Current (Short Circuit) ..... 122 mA
Voltage (200 Ω Load) ..... 8.0 V
Current (200 Ω Load) ..... 42 mA

12V Mode
No Load Voltage (Open Circuit) ..... 17.5 V
No Load Current (Short Circuit) ..... 60 mA
Voltage (200 Ω Load) ..... 10.5 V
Current (200 Ω Load) ..... 52 mA

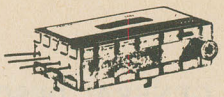
TYPICAL CHARACTERISTICS



Current vs Voltage

UM1285-8 VHF MODULATOR

277-221



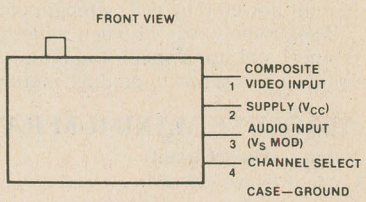
GENERAL DESCRIPTION

The UM1285-8 is a high performance intercarrier vestigial sideband modulator which is primarily intended for use in color TV games, home computer, graphics, teletext and view data adapters. The modulator has a very linear transfer characteristic which ensures good chroma levels and freedom from sync compression and associated frame and line jitter problems, good subcarrier inter modulation performance minimizes the on screen bar pattern due to chroma and sound subcarrier beats.

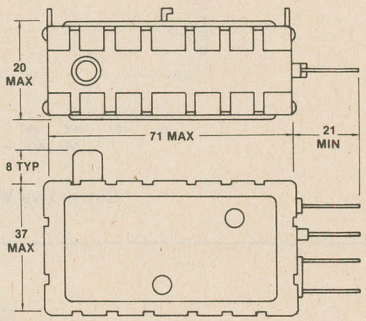
FEATURES

- Compact & low profile
- Rugged & stable
- Good modulation linearity
- Low chroma/sound beat product (55 dB typ)
- Pretuned vision carriers Ch 3, Ch 4
- Pretuned sound subcarrier 4.5 MHz
- Pretuned vestigial sideband filter
- Built-in voltage regulator
- Negative transfer characteristic
- For color application
- 75 ohm output from a standard phono socket

PIN CONNECTION



DIMENSIONAL DIAGRAM



Dimensions in mm

ABSOLUTE MAXIMUM RATINGS

Voltage between Pin 1, 3, 4, and Case Ground ..... – 3.0 to + 15 V
Voltage between Pin 3 and V_{CC} ..... – 3.0 to + 8.0 V
(Refer to table for high voltage application.)
Operating Temperature Range ..... 0 to + 45°C
Storage Temperature Range ..... – 20 to + 70°C

ELECTRICAL CHARACTERISTICS

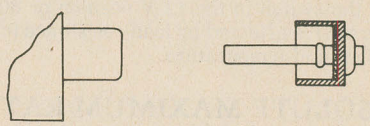
V_{CC} ..... + 5.8 to 6.2 V
(Refer to table for higher supply voltage application.)
RF Output Load 75Ω
Channel 3 Video Carrier ..... 61.25 MHz
Channel 4 Video Carrier ..... 67.65 MHz
Sound Carrier ..... 4.500 MHz
Video Carrier output (Vmod = 2.2 V) ..... 1.5 mVrms
Video Carrier output (Vmod = 2.8 V) ..... 18 dB WRT V_O(HI)
Sound Carrier output ..... 22 dB WRT V_O(HI)
Spurious/Harmonic ..... 30 dB WRT V_O(HI)
Voltage Standing Wave Ratio (CH 3 and CH 4) 1.7
ΔF for Change in Temperature ..... ±10 kHz/°C
ΔF for Change in Temperature ..... ±750 Hz/°C
ΔF for 1 Volt Change in V_{CC} ..... ±30 kHz/V
ΔF for 1 Volt Change in V_{CC} ..... ±5 kHz/V
RF Output Impedance 75Ω
– 3DB Bandwidth (RF)
CH 3 ..... 14 MHz
CH 4 ..... 5.0 MHz
Supply Current ..... 30 mA
Frequency modulating ..... 8 kHz/Volt
Sensitivity Chroma/Sound Beat Level ..... 55 dB WRT V_O(HI)

TABLE

Supply Voltage V_{CC}	Volt	6.0	7.5	9.0	12.0	15.0
Series Resistor R_S	Ohm	0	47	100	180	270

Series resistor with respect to supply voltage

RF OUTPUT SOCKET



Phono Socket Typical Phono Plug

UM1285-5 277-221

TYPICAL CHARACTERISTICS

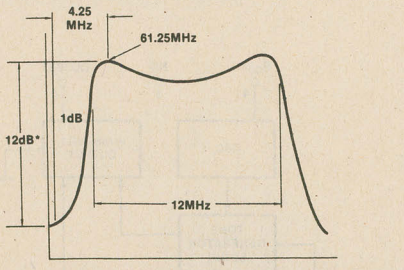
The UM1285-8 is designed to work over a wide range of supply voltage from 6 to 15 V (V_{CC}). A built-in 5.0 V (V_{DD}) voltage regulator is provided to achieve excellent stability against voltage change. A series resistor is recommended in putting between power source and modulator supply input for purpose of current limiting.

Modulation occurs when a positive going voltage is applied to the modulation input (video) pin. The transfer characteristic is negative, that means a positive input causes the RF output to decrease. Peak RF output is specified when the video input is at 2.2 V.

RF channel frequency of Ch 3 or Ch 4 can be selected by connecting channel select pin to ground level (0V) to have Ch 3, or open connection to have Ch 4.

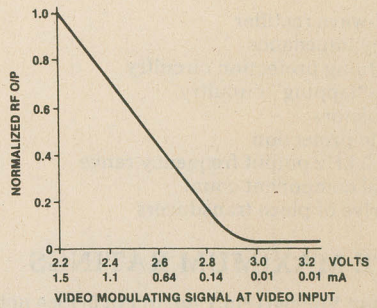
FCC APPROVABLE

The UM1285-8 is FCC approvable due to its very low radiation, stabilized carrier oscillators and vestigial side bank filter which ensures all side band components outside FCC limits are greater than 30 dB down.



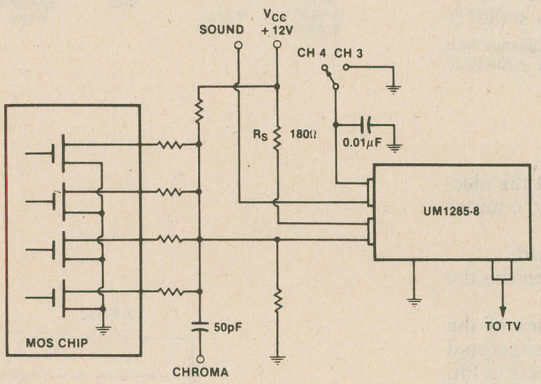
*Note: Subcarriers are > 18dB down wrt carrier at input to bandpass filter giving maximum out of band level of < −30dB wrt carrier.

Typical Bandpass Filter Response

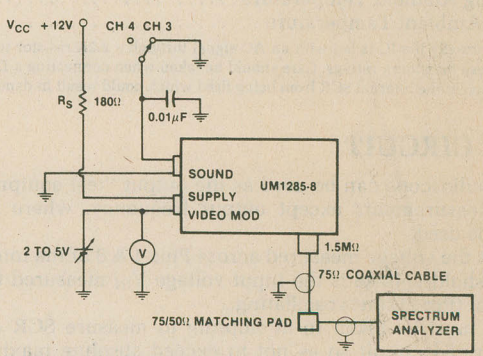


Typical Transfer Characteristic

TYPICAL APPLICATIONS



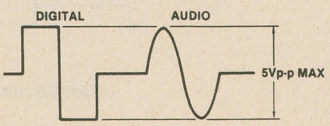
Typical Application



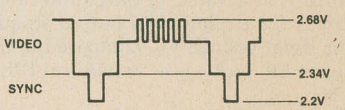
Note: 1. In case of testing with 50Ω I/P spectrum analyzer, matching pad 75/50Ω (attenuation 10dB) shound be employed.
2. Standard RF coaxial cable should be 1.5 meters long and 75Ω characteristic impedance.

Test Circuit

TYPICAL INPUT WAVEFORMS

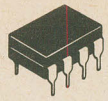


Sound I/P Setup



Modulated Input Voltage Setup

TCM1512A 276-1302 RING DETECTOR/DRIVER

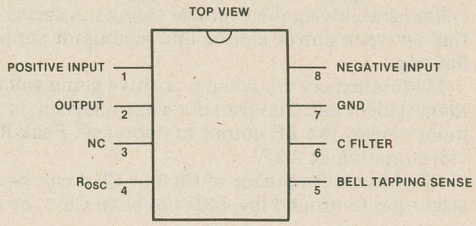


GENERAL DESCRIPTION

The TCM1512A integrated circuit is designed for use as an alerting device in the line powered telephone. The IC (with a minimum of external components) is powered and activated by the telephone line's AC "ring" voltage to generate a signal suitable for driving piezo-electric "sound disc" transducers. In a typical telephone application this AC ring voltage can vary from 40 to 150 V_{RMS} over a frequency range of 14 to 68 Hz. The output signal is a square wave alternating between two frequencies in a ratio 1.14:1; and with the average of these two frequencies set at 1250 Hz, a "warble" rate or shift rate of approximately 10 Hz.

During standby (prior to activation) the ringer presents an impedance of 100K or greater to prevent any interference with parallel "offhook" telephones transmitting DTMF or voice frequencies. The IC is designed to handle lightning strikes on the line of 1500 V, 200 μsec duration. In addition, dial pulses from parallel phones are ignored so a false ringing of the bell (tapping) won't occur.

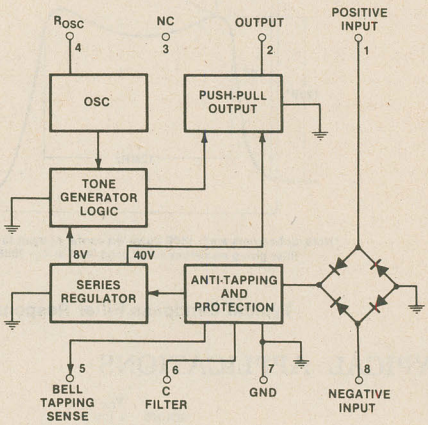
PIN CONNECTION



FEATURES

- On-chip full-wave rectifier
- High standby impedance
- Built-in lightning protection circuitry
- Built-in anti-"tapping" circuitry
- Built-in regulators
- Built-in static protection
- 0.8 through 2 kHz output frequency range
- Low external component count
- Push-pull drive of piezo transducers

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

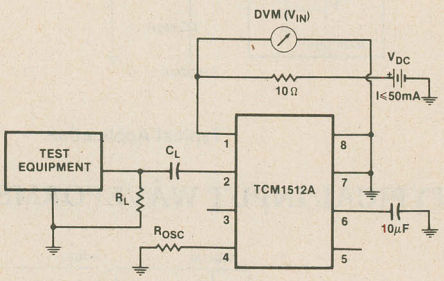
Continuous Input Voltage (Pin 1 ref. to Pin 8) (See note) ..... 70 V
Continuous V_{CC} Supply (Pin 6 ref. to Pin 7) (See note) ..... 63 V
Package Power Capability @25°C ..... 1 W
Surge SCR On-STate Current (On-Time ≤ 200 μsec) ..... 0.9 A.
Continuous Input Current (with SCR Triggered) (See note) ..... 0.5 A_{RMS}.
Operating Ambient Temperature ..... −20 to +70°C
Storage Ambient Temperature ..... −40 to +150°C

NOTE: Normally the IC is fed with an AC signal through a 2.2K resistor to guarantee compliance with these maximum ratings. Care should be taken when connecting a DC power supply to the IC to prevent the internal SCR from being fired which could result in damage to the IC.

TEST CIRCUIT

An oscilloscope can be used as the output "test equipment" for all the electrical measurements except output frequency, where a frequency counter should be used.

1. V_{IN} is the voltage measured across Pins 1 & 8 of the integrated circuit.
2. Threshold voltage is the input voltage V_{IN} measured the instant before the output (Pin 2) starts oscillating.
3. Care must be taken in attempting to measure SCR characteristics of the integrated circuit so as not to exceed absolute maximum. It is suggested that a curve tracer be used across Pins 1 & 8 with capacitor connection Pin 6 shorted to Pin 7 to simulate a standby transient effect of a discharged 10 μF filter capacitor.
4. DC output currents are measured in the steady state. Peak output current would normally be greater than specified.
5. The output frequency is measured across R_L using a frequency counter. The frequency counter measures and displays the average frequency of the output tones F_{AVG} (where F_{AVG} = the average of the high frequency of the low frequency which is integrated by the counter over a long period of time).
6. Oscillator drift is the deviation in output frequency due to change in temperature T_A or input voltage V_{IN} compared to the output frequency at T_A = 25°C and V_{IN} = 30 V. R_{OSC} is varied until the average output frequency F_{AVG} = 1250 Hz.
7. For most tests, Pin 5 is left open. Where specified, Pin 5 is activated by connecting a 2.2K resistor across Pins 5 & 6.



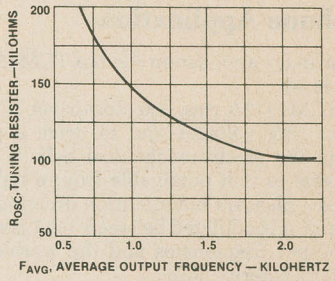
Test Circuit

TCM1512A 276-1302

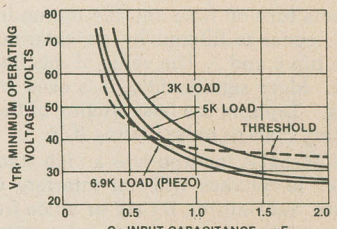
TYPICAL CHARACTERISTICS

This first graph shows the typical average output frequency vs. oscillator tuning resistor (R_{OSC}). The curve shows the general trend that the IC's follow; however, the values will differ from IC to IC. The curve should not be used as an accurate design tool since IC's could vary more than ± 10% from the values given in this graph.

The second graph shows the minimum operating voltage at tip and ring (20 Hz) vs. input capacitance C1 as a function of load resistance. The dashed curve marked "threshold" shows the voltage necessary at tip and ring to produce a voltage between pin 6 and 7 large enough to trip an internal switch and start the output oscillating. However, depending on the load and input capacitance, the minimum operating voltage could be larger than the threshold voltage. The threshold voltage can turn the IC on for an instant until the load drains the 10 μF capacitor across pins 6 and 7 and then the IC would turn off again. Depending on R_{LOAD} and C1, the minimum operating voltage could be the true threshold voltage.



Tuning Resistor vs Average Output Frequency



Minimum Operating Voltage vs Input Capacitance

TYPICAL APPLICATIONS

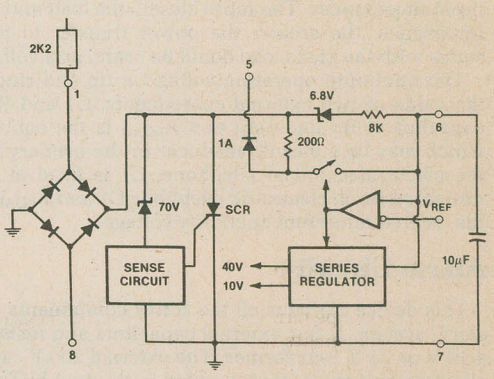
Input Circuitry

The TCM1512A has built-in circuitry to avoid "tapping," a false triggering due to transients. The IC is kept "OFF" (in standby) until the incoming signal has charged the capacitor on pins 6 and 7 to a threshold of approximately 8 volts through an internal zener and 8K resistor.

Connecting pin 5 and pin 6 bypasses the internal zener and thus reduces the threshold voltage, (V_{IN}). The connection, if made, should be with a resistor of not less than 2K.

The ring detector/driver IC has built-in transient protection circuitry which (with appropriate external circuitry) is designed to handle lightning strikes (1500 V/200 μsec) on a phone line. The IC is made up of a high current SCR triggered by a circuit that senses current (typically 70 mA) through the 70 V on-chip zener. The external 2.2K resistor is a necessary component to dissipate the energy when the SCR is turned on. Therefore, with an external resistor of 2.2K, a voltage transient of 224 V (peak) from tip to ring, will fire the SCR. (2200 Ω × 0.07 A Pk) + 70 V = 224 V (Pk), Note: Caution is required when a DC power supply is connected to the input pins (1 and 8). If the IC is subjected to a transient, it could possibly fire the SCR and would not turn off until the current supplied to it falls below the holding current I_H. The DC power supply provides constant current and would result in IC destruction.

The ring detector/driver IC has a standby impedance of greater than 100K. The IC achieves such a high impedance due to an on-chip series zener which presents a high impedance until its turn-on voltage (6.8V) is reached. However, when the IC reaches its threshold voltage (8V) across pins 6 and 7, an internal switch is closed which bypasses the 6.8 V zener. This allows for more efficient power transfer to the load when the IC is in the operating mode. In the operating mode the IC has an AC impedance determined largely from the output load.

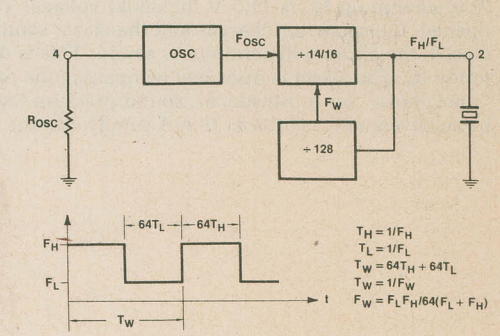


Input Circuitry

Output Tone Operation

The external resistor R_{OSC} sets the frequency of the IC's oscillator. The oscillator frequency F_{OSC} is then divided by a divide-by-14 counter for the high frequency F_H and a divide-by-16 counter for the low frequency F_L. The output frequencies are then divided by a divide-by-128 counter to establish the "warble rate." The warble rate is the alternation between the high frequency F_H and the low frequency F_L. Therefore, by changing the oscillator resistor R_{OSC}, the pitch of the output tones (F_H/F_L) and the warble rate between the tones can be set to the desired value. Oscillator drift is kept to a minimum (−1% to ±0.5%) during varying input voltages and operating temperatures due to an on-chip 10 V regulator and circuit design techniques. Tolerance of the output frequencies (F_H/F_L) from IC to IC are dependent upon IC tolerances and R_{OSC} tolerance and is normally in excess of ± 10%.

Oscillator Stability: It is recommended that on PCB's, R_{OSC} be located close to pin 4 (short lead) and be surrounded by ground plane. Also, pin 3 (N/C) should be grounded. These measures will prevent capacitive coupling from the output to the master oscillator, which may cause oscillator instability.



Output Tone Operation

TCM1512A 276-1302

TYPICAL APPLICATIONS (Cont'd)

Telephone Application

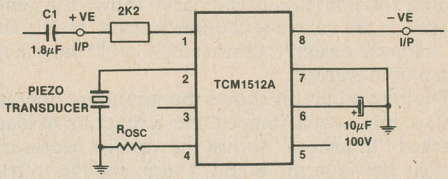
The primary application for the TCM1512A ring detector/driver IC is in the telephone set.

This TCM1512A ring detector/driver IC is designed for use in telephone sets to detect ring voltages and to drive a piezo-ceramic disc transducer, thus replacing the electromechanical bell. It can produce sound with efficiency comparable to that obtainable from a type 500 set. The typical output signal produces a pleasant but attention drawing sound with an average frequency of 1250 Hz. It is modulated between 1172 Hz and 1339 Hz at a 9.8 Hz warble rate. These output frequencies and the warble rate are adjustable by varying the value of the external R_{OSC}.

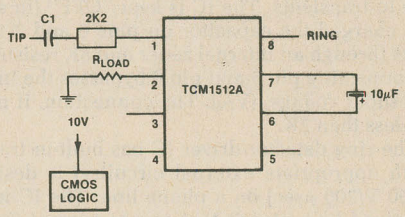
The network formed by the 1.8 μF DC blocking capacitor, the 2.2K current limiting resistor, and the diode full wave bridge supply the IC power from the phone lines. The 1.8 μF capacitor is "standard" with U.K. mechanical telephones and normally part of the hybrid network. The value of the capacitor (C1) affects turn-on time and the minimum input voltage. The incoming rectified AC signal is filtered by an external 10 μF/100 V capacitor connected between pin 6 and 7. The value of this filter capacitor affects the turn-on time of the IC. More significantly, it is used with internal IC circuitry to suppress "tapping." Tapping is a false ringing of the bell due to pulses on the phone line from rotary dials or pulse dialing IC's.

The TCM1512A incorporates a high standby input impedance to assure that "on-hook" telephones will not interfere with parallel (extension) "off-hook" telephones transmitting DTMF or voice frequency signals. Industry standards specify < 100K for voice frequencies (700 Hz - 1.6 kHz) for input voltages up to 3 V_{RMS}. The impedance for operating voltages (during ring) is specified to be < 8K. The TCM1512A meets both of these requirements. The DC blocking capacitor (C1) and the filter capacitor could modify the value of the ringer input impedances. The more closely the load and IC impedance match the line impedance, the greater the power transfer to the load. A potentiometer in series with the piezo load could be useful as a volume control.

The minimum operating voltage at tip and ring can be altered by changing the value of two external components, C1 and R_{LOAD}. C1 is the DC blocking capacitor at tip and ring and R_{LOAD} is the equivalent resistance of the load which may be a piezo transducer or the primary winding of a transformer. In the electromechanical telephone, C1 is fixed at 1.8 μF. However, if one is designing an all electronic telephone C1 and R_{LOAD} could be selected to achieve the desired minimum operating voltage.



Telephone Application of Ring Detector/Driver

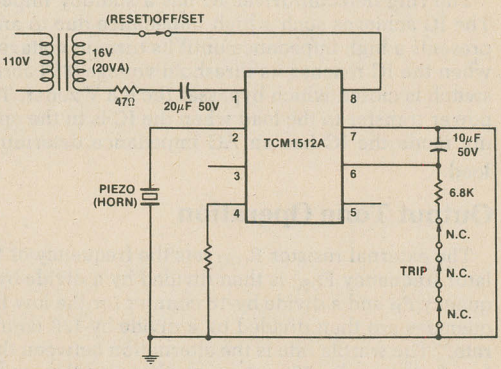


Input/Output Circuitry

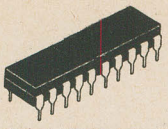
Alarm Circuit

This device contains all the active components necessary to build a security alarm system. A few external capacitors and resistors are required, along with a 16 V or 24 V transformer. The external 20 μF capacitor stores voltage during alternate half-cycles that is added to the next half-cycle's voltage to generate 30 V (Pk) across pins 6 and 7. The voltage doubler allows the IC to turn on with lower supply voltages than are normally required.

The IC is in standby (Off) when the "trip" switches are in their normally closed position. The 6.8K resistor doesn't allow the 10 μF capacitor (pins 6 and 7) to charge up to its 11.5 V threshold voltage. The instant the trip switch is opened, the capacitor charges and the alarm sounds. Even if the trip switch is closed, the alarm will continue to sound. This is due to a latch circuit internal to the IC. The alarm is disarmed by opening the reset/set switch. when using a "piezo horn" for a transducer, sound pressure levels of 105 dB or greater can be achieved with as little as 10 mA supply current.



Alarm Circuit



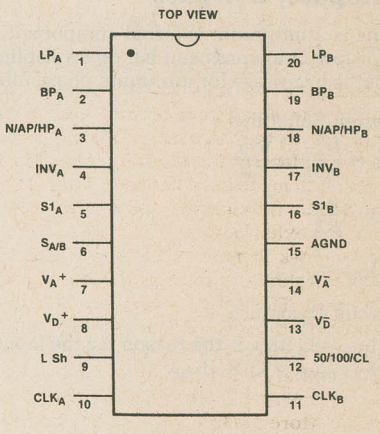
UNIVERSAL MONOLITHIC DUAL SWITCHED CAPACITOR FILTER

MF10
276-2329

GENERAL DESCRIPTION

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

PIN CONNECTION



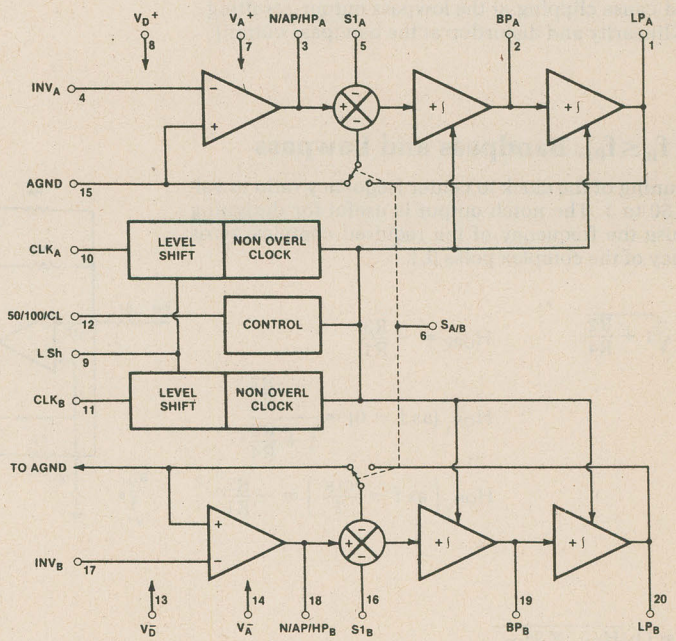
FEATURES

- Low cost
- 20-pin 0.3″ wide package
- Easy to use
- Clock to center frequency ratio accuracy=0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_o \times Q$ range up to 200 kHz
- Operation up to 30 kHz

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7V
Power Dissipation 500mW
Operating Temperature ..... 0 to 70°C
Storage Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

BLOCK DIAGRAM



MF10 276-2329

TYPICAL APPLICATIONS

Mode 1A: Non-Inverting Bandpass, Inverting Bandpass, Lowpass

This is a minimum external component configuration (only 2 resistors) useful for low Q lowpass and bandpass applications. The non-inverting bandpass output is necessary for minimum phase filter designs.

Design Equations

$f_o = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = -1$

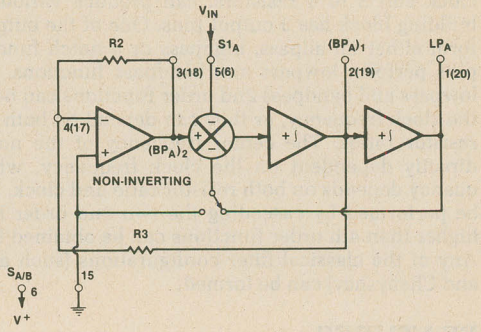
$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

Circuit Dynamics

$H_{OBP_1} = Q$ (this is the reason for the low Q recommendation)

$H_{OLP\,(peak)} = Q \times H_{OLP}$



Mode 1A

Mode 1: Notch, Bandpass and Lowpass

With the addition of just one more external resistor, the output dynamics are improved over Mode 1A to allow bandpass designs with a much higher Q. The notch output features equal gain above and below the notch frequency.

Design Equations

$f_o = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$f_{notch} = f_o$

$Q = \frac{R3}{R2}$

$H_{OLP} = -\frac{R2}{R1}$

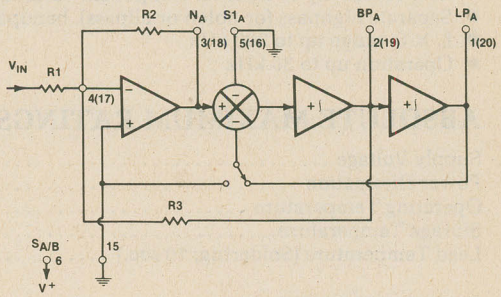
$H_{OBP} = -\frac{R3}{R1}$

$H_{ON} = -\frac{R2}{R1}$ as $f \to 0$ and as $f \to \frac{f_{CLK}}{2}$

Circuit Dynamics

$H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$

$H_{OLP(peak)} = Q \times H_{OLP}$ (if the DC gain of the LP output is too high, a high Q value could cause clipping at the lowpass output resulting in gain non-linearity and distortion at the bandpass output).



Mode 1

Mode 2: Notch (with $f_n \leq f_0$), Bandpass and Lowpass

This configuration allows tuning of the clock to center frequency ratio to values greater than 100 to 1 or 50 to 1. The notch output is useful for designing elliptic highpass filters because the frequency of the required complex zeros (f_{notch}) is less than the frequency of the complex poles (f_o).

Design Equations

$f_o = \frac{f_{CLK}}{100}\sqrt{1+\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50}\sqrt{1+\frac{R2}{R4}}$

$f_n = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \sqrt{1+\frac{R2}{R4}} \times \frac{R3}{R2}$

$H_{OLP} = \frac{-\frac{R2}{R1}}{1+\frac{R2}{R4}}$

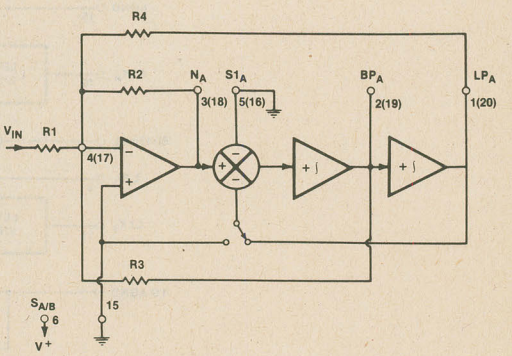
$H_{OBP} = -\frac{R3}{R1}$

H_{ON_1} (as $f \to 0$) $= \frac{-\frac{R2}{R1}}{1+\frac{R2}{R4}}$

$H_{ON_2}\left(\text{as } f \to \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

Circuit Dynamics

$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON_2}} = Q\sqrt{H_{ON_1} \times H_{ON_2}}$



Mode 2

TYPICAL APPLICATIONS (Cont'd)

Mode 3: Highpass, Bandpass and Lowpass

This configuration is the classical state variable filter implemented with only 4 external resistors. This is the most versatile mode of operation, since the clock to center frequency ratio can be externally tuned either above or below the 100 to 1 or 50 to 1 values. The circuit is suitable for multiple stage Chebyshev filters controlled by a single clock.

Design Equations

$$f_o = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}} \qquad H_{OBP} = -\frac{R3}{R1}$$

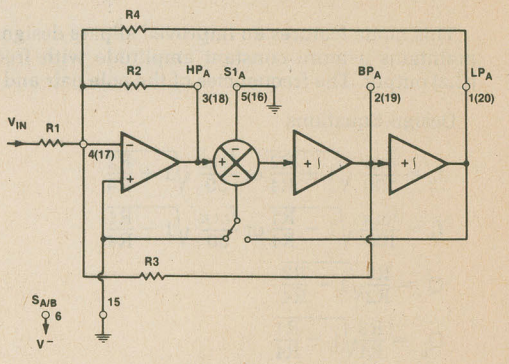
$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2} \qquad H_{OLP} = -\frac{R4}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

Circuit Dynamics

$$H_{OHP} = H_{OLP}\left(\frac{R2}{R4}\right) \qquad H_{OBP} = Q\sqrt{H_{OHP} \times H_{OLP}}$$

$$H_{OLP\,(peak)} = Q \times H_{OLP} \qquad H_{OHP\,(peak)} = Q \times H_{OHP}$$



Mode 3

Mode 3A: Highpass, Bandpass, Lowpass and Notch

A notch output is created from the circuit of Mode 3 by summing the highpass and lowpass outputs through an external op amp. The ratio of the summing resistors R_h and R_l adjusts the notch frequency independent of the center frequency. For elliptic filter designs, each stage combines a complex pole pair (at f_o) with a complex zero pair (at f_{notch}) and this configuration provides easy tining of each of these frequencies for any response type. When cascading several stages of the MF10 the external op amp is needed only at the final output stage. The summing junction for the intermediate stages can be the inverting input of the MF10 internal op amp.

Design Equations

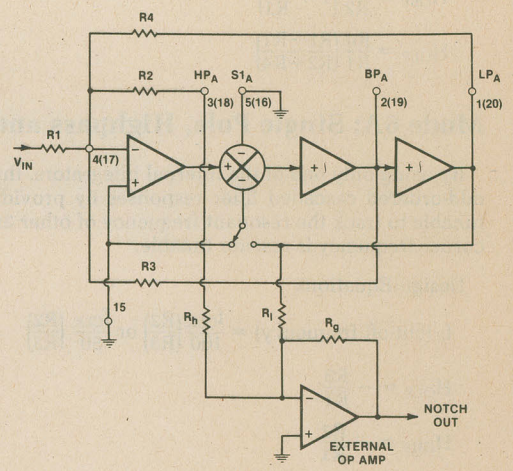
$$f_o = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}} \qquad H_{OBP} = -\frac{R3}{R1}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2} \qquad H_{ON}\,(\text{at } f = f_o) = \left|Q\left(\frac{R_g}{R_l}H_{OLP} - \frac{R_g}{R_h}H_{OHP}\right)\right|$$

$$f_{notch} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}} \qquad H_{ON_l}\,(\text{as } f \to 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{OHP} = -\frac{R2}{R1} \qquad H_{ON_h}\left(\text{as } f \to \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h} \times H_{OHP}$$

$$H_{OLP} = -\frac{R4}{R1}$$



Mode 3A

Mode 4: Allpass, Bandpass and Lowpass

Utilizing the $S1_A$ ($S1_B$) terminal as a signal input, an allpass function can be obtained. An allpass can provide a linear phase change with frequency which results in a constant time delay. This configuration restricts the gain at the allpass output to be unity.

Design Equations

$$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \qquad H_{OAP} = -\frac{R2}{R1} = -1$$

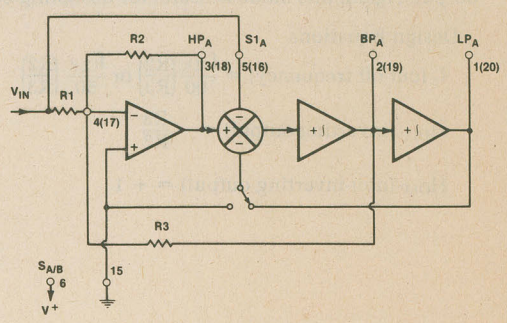
f_z (frequency of complex zero pair) $= f_o$ $\qquad H_{OLP} = -\left(\frac{R2}{R1} + 1\right) = -2$

$$Q = \frac{R3}{R2} \qquad H_{OBP} = -\left(1 + \frac{R2}{R1}\right)\frac{R3}{R2} = -2\frac{R3}{R2}$$

$$Q_z\,(\text{Q of complex zero pair}) = \frac{R3}{R1}$$

Circuit Dynamics

$$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)Q$$



Mode 4

MF10 276-2329

TYPICAL APPLICATIONS (Cont'd)

Mode 5: Complex Zeros (C.z), Bandpass and Lowpass

This mode features an improved allpass design over that of Mode 4, in that it maintains a more constant amplitude with frequency at the complex zeros (C.z) output. The frequencies of the pole pair and zero pair are resistor tunable.

Design Equations

$$f_o = \frac{f_{CLK}}{100}\sqrt{1+\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{1+\frac{R2}{R4}}$$

$$f_z = \frac{f_{CLK}}{100}\sqrt{1-\frac{R1}{R4}} \text{ or } \frac{f_{CLK}}{50}\sqrt{1-\frac{R1}{R4}}$$

$$Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$$

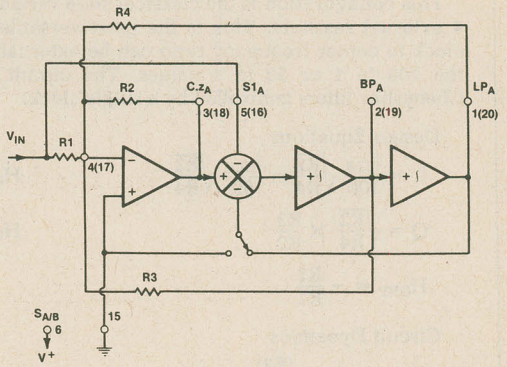
$$Q_z = \frac{R3}{R1}\sqrt{1-\frac{R1}{R4}}$$

$$H_{O(C.z)} \text{ as } f \to 0 = \frac{R2(R4-R1)}{R1(R2+R4)}$$

$$H_{O(C.z)} \text{ as } f \to \frac{f_{CLK}}{2} = \frac{R2}{R1}$$

$$H_{OBP} = \frac{R3}{R2}\left(1+\frac{R2}{R1}\right)$$

$$H_{OLP} = \frac{R4}{R1}\left(\frac{R2+R1}{R2+R4}\right)$$



Mode 5

Mode 6A: Single Pole, Highpass and Lowpass

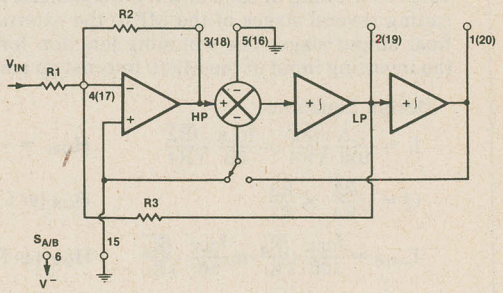
By using only one of the internal integrators, this mode is useful for creating odd-ordered cascaded filter responses by providing a real pole that is clock tunable to track the resonant frequency of other 2nd order MF10 sections. The corner frequency is resistor tunable.

Design Equations

$$f_c \text{ (cut-off frequency)} = \frac{f_{CLK}}{100}\left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50}\left(\frac{R2}{R3}\right)$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$



Mode 6A

Mode 6B: Single Pole Lowpass (Inverting and Non-Inverting)

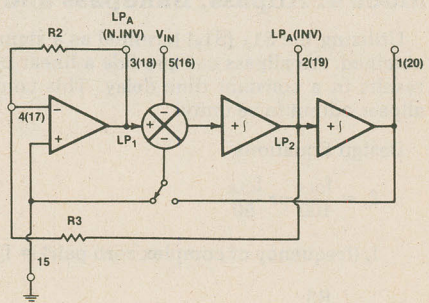
This mode utilizes only one of the integrators for a single pole lowpass, and the input op amp as an inverting amplifier, to provide non-inverting lowpass output. Again, this mode is useful for designing odd-ordered lowpass filters.

Design Equations

$$f_c \text{ (cut-off frequency)} = \frac{f_{CLK}}{100}\left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50}\left(\frac{R2}{R3}\right)$$

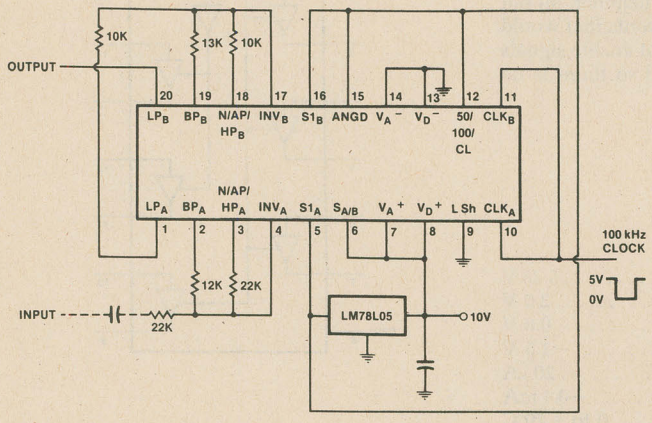
$$H_{OLP} \text{ (inverting output)} = -\frac{R3}{R2}$$

$$H_{OLP} \text{ (non-inverting output)} = +1$$

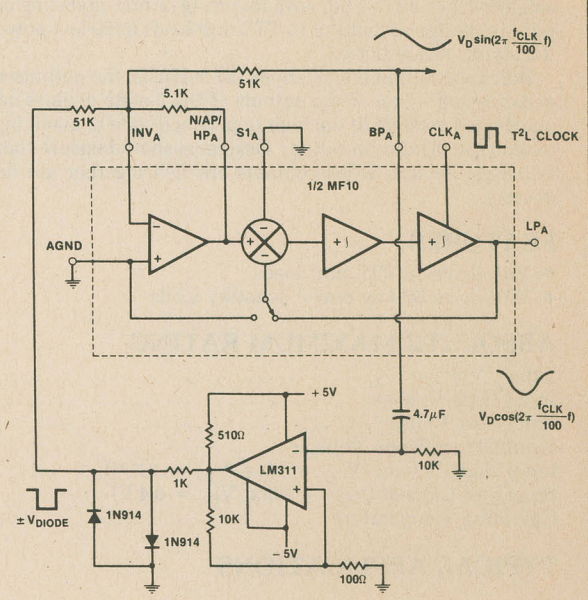


Mode 6B

TYPICAL APPLICATIONS (Cont'd)



Only 6 resistors required for this 4th order, 1 kHz Butterworth lowpass filter. This example also illustrates single-supply biasing.

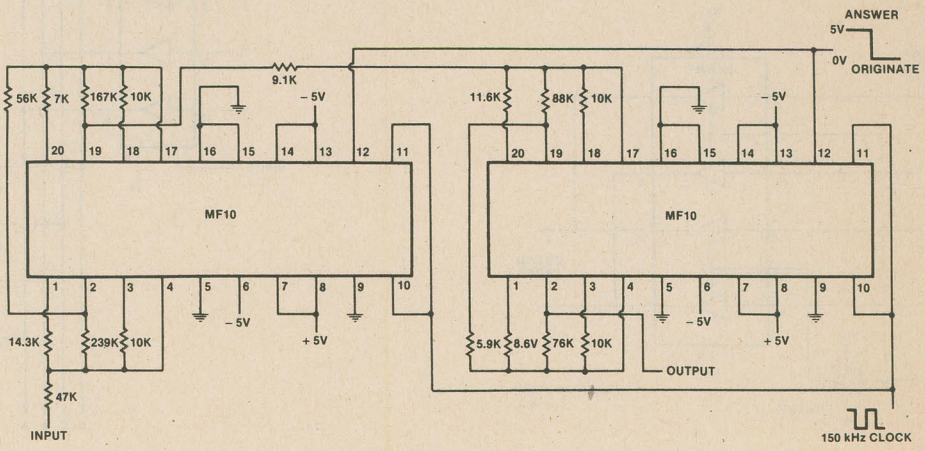


Generating Quadrature Sinewaves from a T²L Clock

300 Baud, Full-Duplex Modem Filter

Finally, as a graphic illustration of the simplicity of filter implementation using the MF10, this is a complete 300 baud, full-duplex modem filter. The filter is an 8th order, 1 dB ripple Chebyshev bandpass which functions as both an 1170 Hz originate filter and a 2125 Hz answer filter. Control of answer or originate operation is set by the logic level at the 50/100/CL input so that only one clock frequency is required. The overall filter gain is 22 dB.

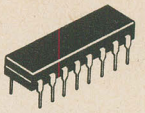
Construction of this filter on a printed circuit board would obviously be more compact than an RC active filter approach and much more cost effective for the level of precision required. An even more attractive implementation from a space savings point of view would be a hybrid circuit approach. A film resistor array connecting to two MF10 die could produce the entire filter in one package requiring only 7 external connections for input, output, supplies, etc.



Complete Full-Duplex 300 Baud Modem Filter

74LS367
276-1835

3-STATE HEX BUFFER



GENERAL DESCRIPTION

This device is a high speed hex buffer with 3-state outputs. It is organized as a single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL unit loads or 60 low power schottky loads when the enable ($\overline{E}$) is LOW.

When the output enable input ($\overline{E}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that output enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

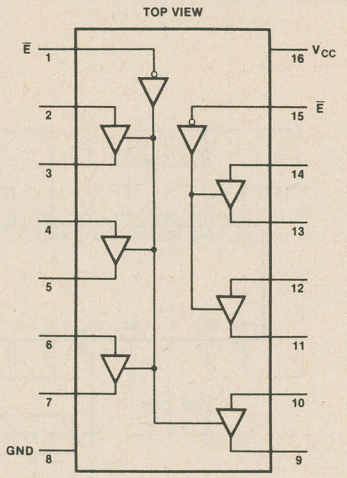
FEATURES

- Will drive 15 TTL unit loads
- Will drive 60 low power schottky loads

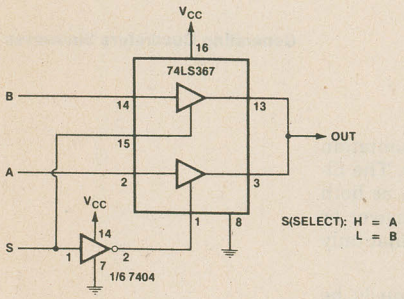
ABSOLUTE MAXIMUM RATING

Supply Voltage V_{CC}	5.25 V
Input High Voltage	2.0 V
Input Low Voltage	0.8 V
Input Clamp Diode Voltage	−1.5 V
Input High Current (V_{CC} = Max., V_{IN} = 2.7 V)	20 μA
Input Low Current (V_{CC} = Max., V_{IN} = 0.4 V)	−0.4 mA
Operating Temperature	0 to +70°C

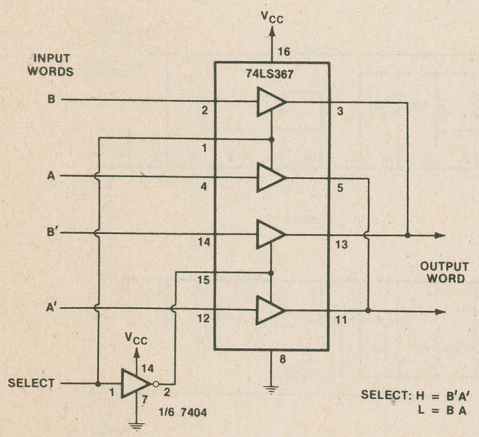
PIN CONNECTION



TYPICAL APPLICATIONS



1-of-2 Data Selector

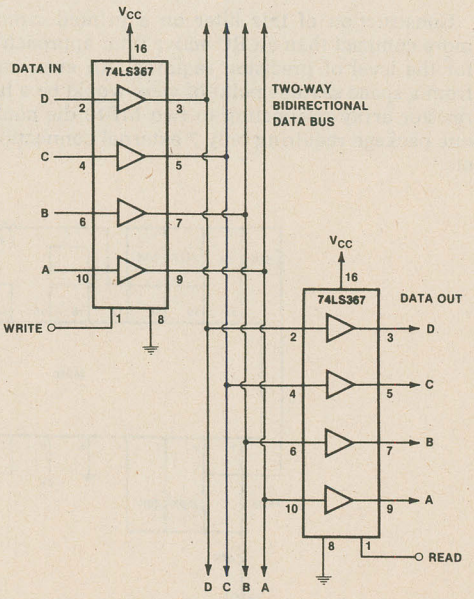


1-of-2 Data Selector

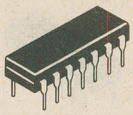
TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance



Bidirectional Data Bus



QUAD TWO-INPUT NAND GATE

7400
276-1801

GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipiation. It provides the basic functions used in the implementation of digital integrated circuit systems.

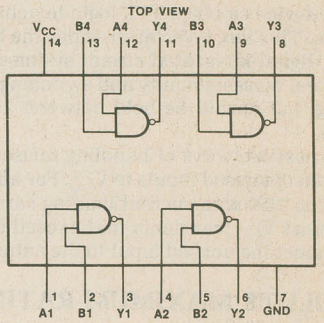
For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways at handling unused inputs are:

(1) Connect unused inputs to V_{CC}. For all multi-emitter conventional TTL inputs, A 1 to 10K ohm current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

(2) Connect the unused input to the output of an unused gate that is forced high.

PIN CONNECTION



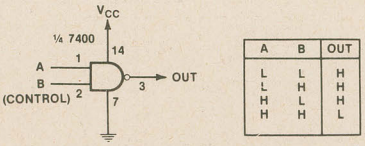
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	5.25 V
Input High Voltage	2.0 V
Input Low Voltage	0.8 V
Input Clamp Diode Voltage (V_{CC} = 5.0 V, I_{IN} = − 12 mA)	− 1.5 V
Input High CUrrent (V_{CC} = Max., V_{IN} = 2.4 V)	40 μA
Input Low Current (V_{CC} = Max., V_{IN} = 0.4 V)	− 1.6 mA
Operating Temperature	0 to + 70°C

TRUTH TABLE

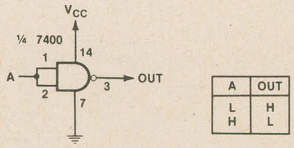
$Y = \overline{AB}$

TYPICAL APPLICATIONS



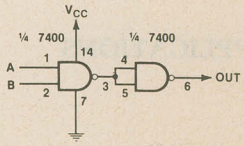
A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

Control Gate



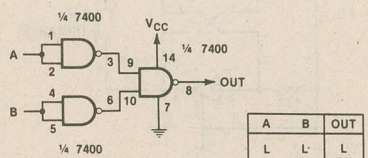
A	OUT
L	H
H	L

Inverter



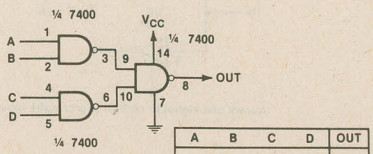
A	B	OUT
L	L	L
L	H	L
H	L	L
H	H	H

AND Gate



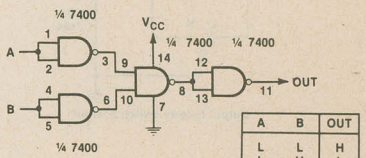
A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	H

OR Gate



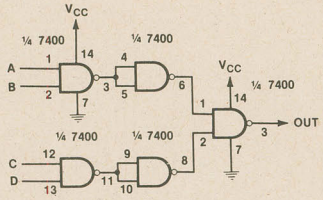
A	B	C	D	OUT
X	X	H	H	H
H	H	X	X	H
H	H	H	H	H

AND-OR Gate



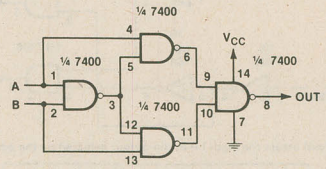
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

NOR Gate



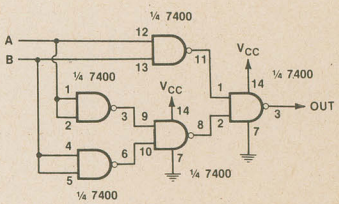
A	B	C	D	OUT
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

4-Input NAND Gate



A	B	OUT
L	L	L
L	H	H
H	L	H
H	H	L

Exclusive-OR Gate

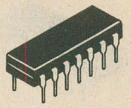


A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	H

Exclusive-NOR Gate

7404
276-1802

HEX INVERTER



GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipation. This hex inverter provides the basic functions used in the implementation of digital integrated circuit systems.

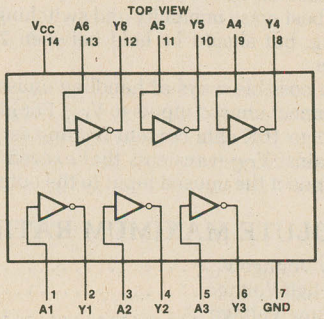
For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

(1) Connect unused inputs to V_{CC}. For all multi-emitter conventional TTL inputs, A 1 to 10K ohm current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

(2) Connect the unused input to the output of an unused gate that is forced high.

PIN CONNECTION



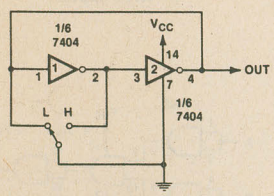
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	5.25 V
Input High Voltage	2.0 V
Input Low Voltage	0.8 V
Input Clamp Diode Voltage (V_{CC} = 5.0 V, I_{IN} = − 12 mA)	− 1.5 V
Input High Current (V_{CC} = Max., V_{IN} = 2.4 V)	40 μA
Input Low Current (V_{CC} = Max., V_{IN} = 0.4 V)	− 1.6 mA
Operating Temperature	0 to + 70°C

TRUTH TABLE

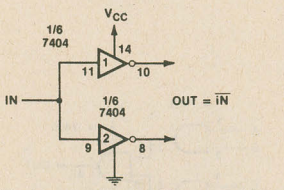
$Y = \overline{A}$

TYPICAL APPLICATIONS



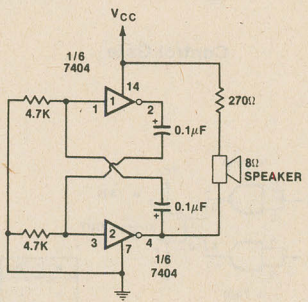
Output follows switch position.

Bouncefree Switch



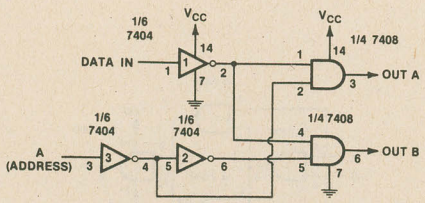
Allows one signal to control two or more inputs.

Universal Expander



Output tone is 4kHz.

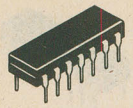
Audio Oscillator



This circuit steers the input bit to the output selected by the address.

DATA	ADDRESS	OUT A	OUT B
L	L	L	H
H	L	H	H
L	H	H	L
H	H	H	H

1-of-2 Demultiplexer



QUAD TWO-INPUT AND GATE

7408
276-1822

GENERAL DESCRIPTION

This device employs TTL logic to achieve high speed at moderate power dissipation. These gates provide the basic functions used in the implementation of digital integrated circuit systems.

For best noise immunity and switching speed, unused inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways at handling unused inputs are:

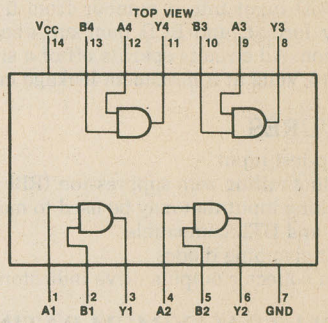
(1) Connect unused inputs to V_{CC}. For all multi-emitter conventional TTL inputs, a 1 to 10K ohm current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

(2) Connect the unused input to the output of an unused gate that is forced high.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} ..... 5.25 V
Input High Voltage ..... 2.0 V
Input Low Voltage ..... 0.8 V
Input Clamp Diode Voltage (V_{CC} = 5.0 V, I_{IN} = − 12 mA) ..... − 1.5 V
Input High Current (V_{CC} = Max., V_{IN} = 2.4 V) ..... 40 μA
Input Low Current (V_{CC} = Max., V_{IN} = 0.4 V) ..... − 1.6 mA
Operating Temperature ..... 0 to + 70°C

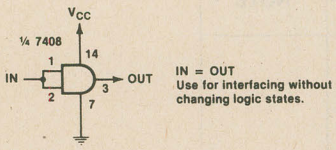
PIN CONNECTION



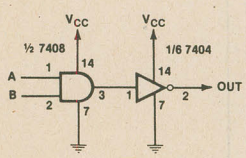
TRUTH TABLE

Y=AB

TYPICAL APPLICATIONS

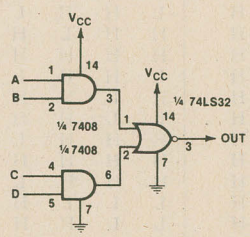


AND Gate Buffer



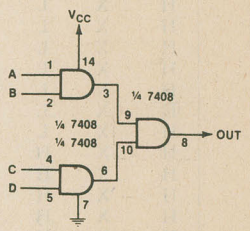
A	B	OUT
L	L	H
L	H	H
H	L	H
H	H	L

NAND Gate



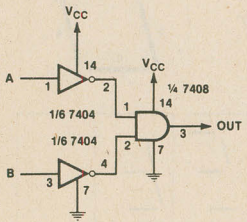
A	B	C	D	OUT
X	X	X	X	H
L	L	X	X	L
X	X	L	L	L

AND-OR-Invert Gate



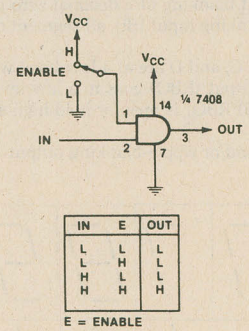
A	B	C	D	OUT
H	H	H	H	H
X	X	X	X	L

4-Input AND Gate



A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

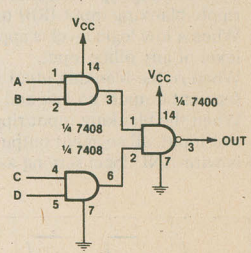
NOR Gate



IN	E	OUT
L	L	L
L	H	L
H	L	L
H	H	H

E = ENABLE

Digital Transmission Gate

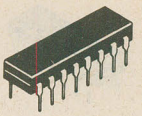


A	B	C	D	OUT
H	H	H	H	L
X	X	X	X	H

4-Input NAND Gate

7447
276-1805

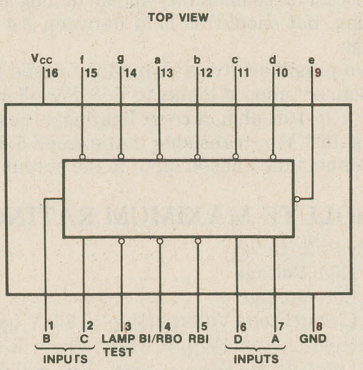
BCD TO SEVEN-SEGMENT DECODER/DRIVER



GENERAL DESCRIPTION

This versatile binary-coded-decimal 7-segment display driver fulfills a wide variety of requirements for most active high (common cathode) and active low (common anode) light emitting diodes (LED) or lamp displays. It fully decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format, and BCD numbers above 9 into unique patterns that verify operation. All circuits operate off of a single 5.0V supply. The output will withstand 15 Volts at a maximum leakage current of 250μA.

PIN CONNECTION



FEATURES

- Lamp-test input
- Leading railing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible
- Input clamping diodes
- Open collector outputs drive indicators directly

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} ..... 4.75 – 5.25 V
Continuous Voltage at Outputs a-g ..... Max. 5.5 V
Logic 1 Input Voltage ..... Min. 2 V
Logic 0 Input Voltage ..... Max. 0.8 V
Logic 0 Output Voltage ..... Max. 0.4 V
Logic 1 Output Voltage at a-g ..... Min. 2.4 V
Logic 1 Output Voltage at BI/RBO ..... Min. 2.4 V
Power ..... 320 mW

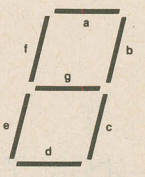
TRUTH TABLE

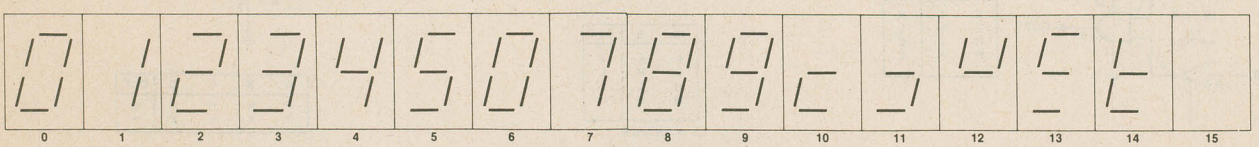
DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	1
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = High Level, L = Low Level, X = Irrelevant

Notes:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 thru 15 are desired. The ripple-blanking input (RB) must be open or high, if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp test input, all segment outputs are high.

† BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

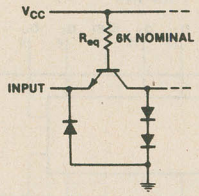




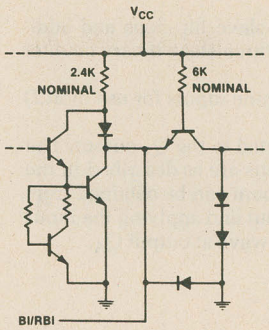
Numerical Designations and Resultant Displays

7447 276-1805

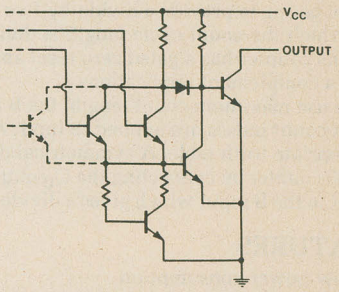
INPUT/OUTPUT EQUIVALENTS



Each Input Except BI/RBO

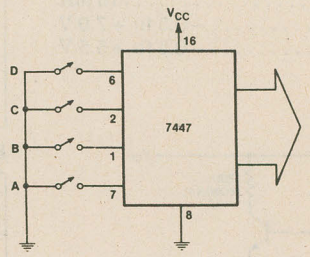


BI/RBO Input

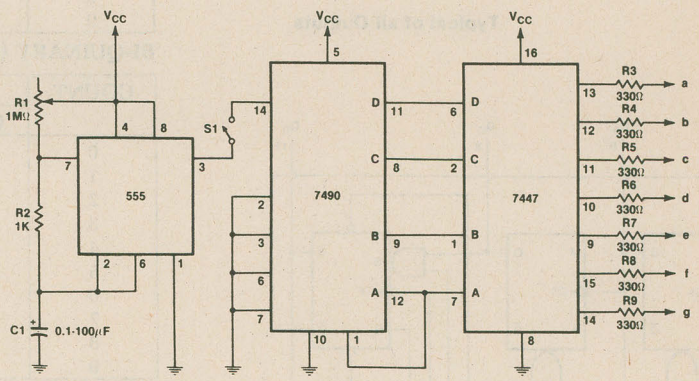


Typical of Outputs a Thru g

TYPICAL APPLICATIONS



Manually Switched Display

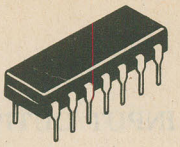


Close S1 to start timing cycle.
Calibrate 555 for 1 pulse (count) per second or 1 count per minute by adjusting R1.

0-9 Second/Minute Timer

7490
276-1808

DIVIDE BY 2 OR 5, BCD COUNTER



GENERAL DESCRIPTION

This monolithic BCD counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

This counter has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

To use maximum count length, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

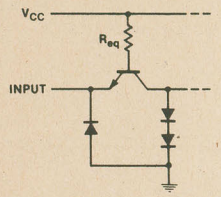
FEATURES

- Low power consumption
- High count rates . . . typically 50MHz
- Choice of counting modes
- Fully TTL and CMOS compatible

ABSOLUTE MAXIMUM RATINGS

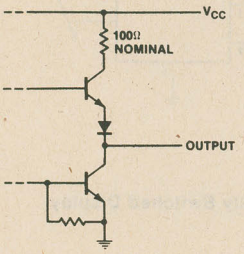
Typical Power Dissipation	145 mW
Count Frequency	42 MHz
High Level Input Voltage (Min)	2 V
Low Level Input Voltage (Max)	0.8 V
High Level Input Current	800 μA
Low Level Output Current (Max)	16 mA
V_{CC} to Ground	−0.5 to +7.0 V
Voltage Applied to Outputs (Output High)	−0.5 to +5.5 V

INPUT/OUTPUT EQUIVALENTS



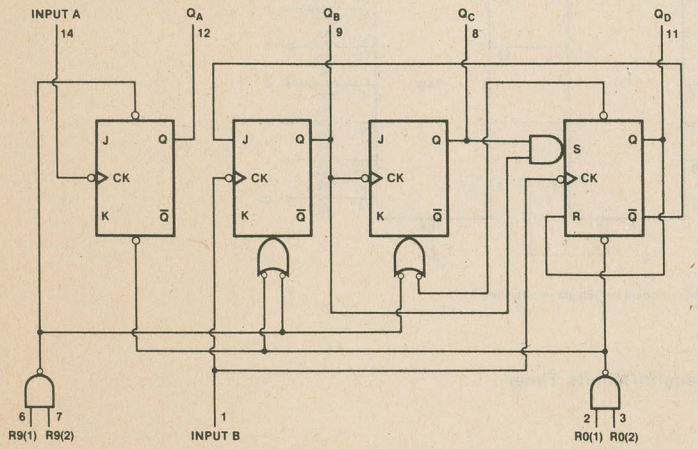
INPUT	R_{eq} NOMINAL
A	2.5K
B	1.25K
ALL RESETS	6K

Each Input

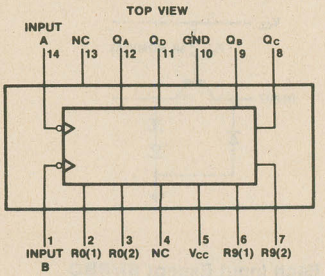


Typical of all Outputs

BLOCK DIAGRAM



PIN CONNECTION



TRUTH TABLES

RESET/COUNT

RESET INPUTS				OUTPUTS			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

BCD COUNT SEQUENCE (See Note A)

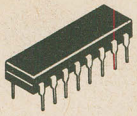
COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUTS			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

L = Low Level
H = High Level

Notes:
(A) Output Q_A is connected to input B for BCD count.
(B) Output Q_D is connected to input A for bi-quinary count.



TONE ENCODER TCM5089

276-1301

GENERAL DESCRIPTION

The TCM5089 is specifically designed for the dual-tone telephone dialing system.

In addition to fixed supply voltage operation, the tone encoder provides negative-true keyboard input, tone inhibit input, stable output tone level, any key depressed feature as well as a single tone inhibit pin.

An inexpensive TV crystal is used to generate eight different audio sinusoidal frequencies.

The tones suitable for dual-tone multi-frequency (DTMF) telephone dialing are digitally synthesized on the chip. The conventional R-2R ladder network is used to provide on-chip digital to analog conversion. The current-to-voltage transformation for D-to-A converter is accomplished by the same operational amplifier which sums up the "low-group" and "high-group" signals.

The waveforms generated in the manner described above have very low total harmonic distortion. Moreover, the frequency stability of this tone encoder complies with standard DTMF specifications without need for any frequency adjustments.

Two voice frequency signals are linearly added to create the dual-tone signal. One frequency is selected from a "low-group" and the other from a "high-group" of frequencies. The "low-group" consists of four frequencies 697, 770, 852, and 941 Hertz. The "high-group" consists of four frequencies 1209, 1336, 1477, and 1633 Hertz.

The number entry is accomplished by a keyboard arranged in a row, column format. In order to select one appropriate row and one appropriate column, a push button corresponding to a digit is pushed. One of the "high-group" frequencies is selected by the active column input and one of the "low-group" frequencies is selected by the active row input. The highest "high-group" frequency of 1633 hertz is not used in standard dual-tone implementation.

The total harmonic and intermodulation distortions of the dual-tone should be less than 10% at the telephone terminals. The frequency tolerance is ±1.0%. TCM5089 tone encoder provides accuracy of less than 0.75%. The "high-group" to "low-group" signal amplitude ratio should be 2.0 ± 1 dB. The above mentioned specifications hold over the safe operating temperature range for either short loop or long loop telephone application.

The TCM5089 is compatible with keyboard as well as electronic inputs. A keyboard diagram is shown in figures 1, and 2. The electronic inputs are shown in figure 3. The standard CMOS operated off the same supply as TCM5089 or open collector TTL can be used for electronic control. The keyboard inputs are standard CMOS with pull-up resistors to the supply voltage V_{DD}. CMOS circuits are capable of realizing resistance up to 1KΩ as a valid key closure; therefore, the precious metals used in keyboard switch contacts can be saved.

In order to generate a particular column tone, the column is connected to V_{SS} and the single tone inhibit is tied to V_{DD}.No tones will result if more than one column is connected to V_{SS}.When one or more rows are connected to V_{SS}, no tones are generated. In order to generate a particular row tone, the row is connected to V_{SS} along with any two column pins. The generation of dual-tones requires connection of a single row and a single column to V_{SS}.

Pin 15 is used to inhibit the generation of single tones. This pin is capable of pulling down to V_{SS} supply voltage. The dual or the single tones are generated as described under keyboard Interface when this pin is connected to V_{DD} supply voltage. When this pin is pulled down to V_{SS} or left floating, all chip functions remain unchanged except for the single tone operation which results in no tone at this voltage level.

The following formula is used to calculate the total harmonic distortion of a single row or a single column.

$$THD = \frac{(\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + V^2_{5f} + \ldots + V^2_{nf}}) \times 100\%}{V_F}$$

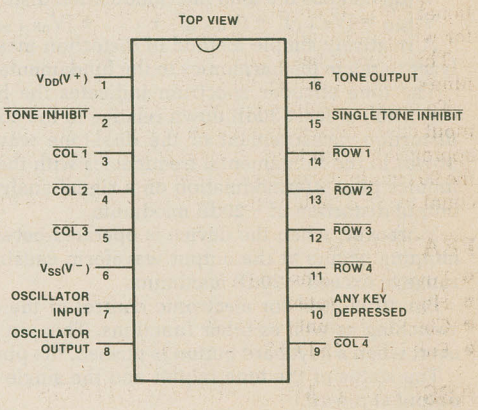
Where V_{2f} is the second harmonic of the fundamental frequency waveform and so on.

The dual-tone total harmonic distortion is given by the following formula:

$$THD = \frac{(\sqrt{V^2_{2R} + V^2_{3R} + \ldots + V^2_{nR} + V^2_{2C} + \ldots V^2_{nC} + V^2_{IMD}}) \times 100\%}{\sqrt{V^2_{FR} + V^2_{FC}}}$$

Where V_{FR} and V_{FC} are the row and column fundamental frequency waveforms, V_{2R} and V_{2C}, etc. are the corresponding harmonics.

PIN CONNECTION



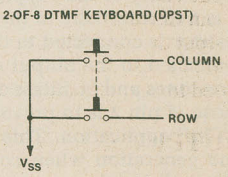


Figure 1—Keyboard Diagram

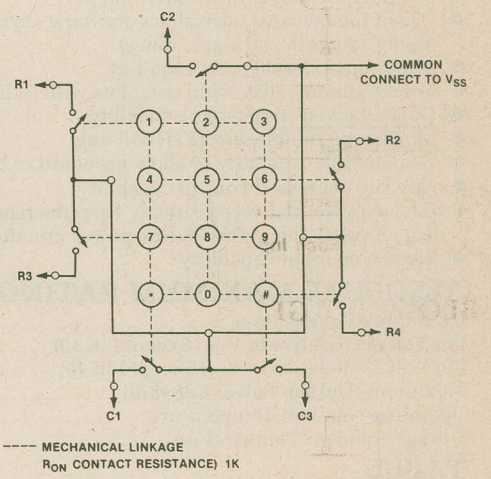


Figure 2—Pushbutton Telephone Keyboard

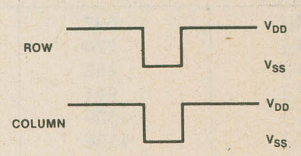


Figure 3—Electronic Inputs

TCM5089 276-1301

GENERAL DESCRIPTION (Cont'd)

V^2_{IMD} denotes the total intermodulation distortion.

$V^2_{IMD} = (V_{R+C})^2 + (V_{R-C})^2 + \ldots + (V_{nR+mC})^2 + (V_{nR-mC})^2$

A relatively simple method of distortion measurement uses a spectrum analyzer to relate the harmonics to the fundamental frequency waveform.

The tone encoder spectrum indicates the harmonics and intermodulation distortion at least 30dB down relative to the column tone. Another method for distortion measurement of the dual-tone waveform is to compare the total power in the fundamental frequencies with the total power in the various harmonics plus intermodulation on a signal analyzer. The TCM5089 provides an output distortion of −20dB maximum.

Moreover, when the device is operated between 3 volts and 3.5 volts, some clipping occurs at the output waveform causing the distortion in this voltage range to exceed −20dB maximum.

Pin 10 is used for electronic control of the transmitter and/or the receiver switching as well as other functions. This pin acts like an open-circuit. However, when a keyboard button is pushed, the pin switches to V_{SS}.

The status of the tone inhibit and the single tone inhibit does not affect the output at pin 10.

The level of the TCM5089's output tone is proportional to the fixed DC supply voltage. In order to increase the temperature stability of the device, operation is usually performed with a regulated supply. The reason being that the temperature stability of the supply voltage can be controlled. The tone output i.e., pin 16 is tied internally to the emitter of an NPN transistor. The collector of this transistor is connected to the V_{DD} supply voltage. The base of this transistor is connected to the output of the on-chip Op Amp used to add the column and row tones and facilitate output level regulations.

The purpose of pin 2 is to prevent tone generation when the keyboard is not used for DTMF application. This pin has a pull-up to V_{DD} voltage supply. It inhibits tone generation when connected to V_{SS}. However, other chip functions remain unchanged.

FEATURES

- Fixed-supply voltage operation
- Minimal standby power requirement
- Use of inexpensive television colorburst crystal (3.579545MHz to provide highly accurate and stable tones)
- Minimum external parts required
- Total harmonic distortion complies with industry standards
- Dual-tone and single-tone capability
- Single tone inhibit selects DTMF only
- Tone inhibit capability to allow keyboard to be used for non-DTMF functions
- Any key depressed control capability
- Device power delivered directly from the telephone lines or small batteries (e.g., 9 volts) due to CMOS low power circuitry
- Electronic input capability

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V_{DD} ..... +13.5 V
Pin Voltage Relative to V_{DD} (Except Pin 10) ..... +0.30 V
Pin Voltage Relative to V_{SS} (Except Pin 10) ..... −0.30 V
Maximum Package Power Capability ..... 1150 mW
Operating Ambient Temperature ..... −30 to +70°C
Storage Ambient Temperature ..... −55 to +150°C

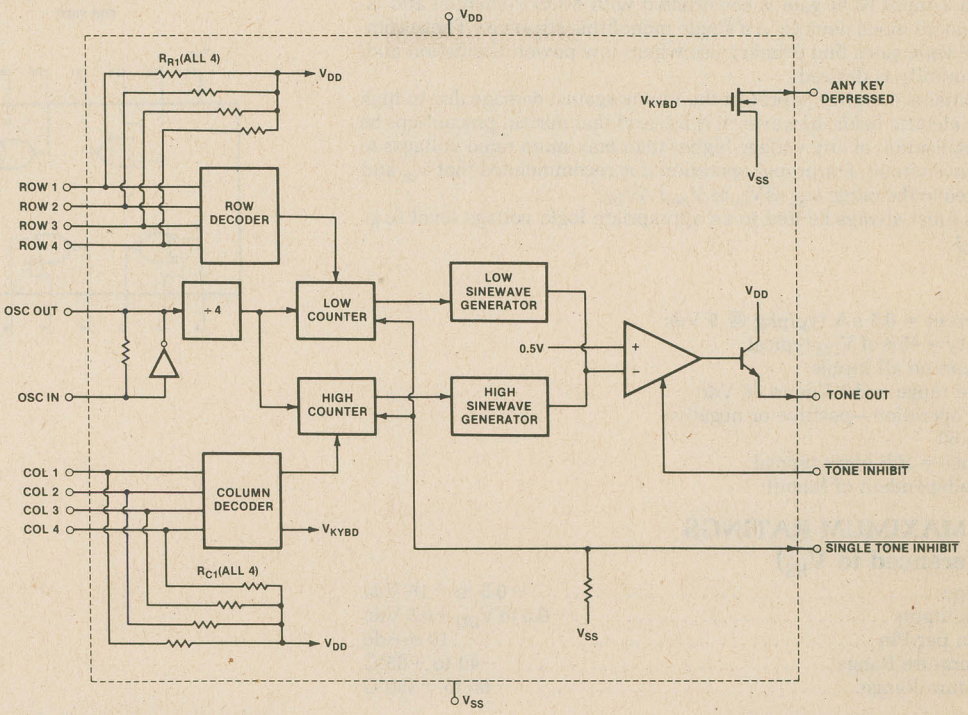
TABLE

Comparison of standard versus actual tones generated by TCM5089 using F = 3.579545 MHz ± .02% crystal oscillator.

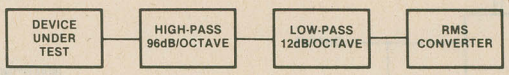
FREQUENCY	STANDARD DTMF	OUTPUT TONE	%ERROR
$f_1(R_1)$	697	701.3	+0.62
$f_2(R_2)$	770	771.4	+0.19
$f_3(R_3)$	852	857.2	+0.61
$f_4(R_4)$	941	935.1	−0.63
$f_5(C_1)$	1209	1215.9	+0.57
$f_6(C_2)$	1336	1331.7	−0.32
$f_7(C_3)$	1477	1471.9	−0.35
$f_8(C_4)$	1633	1645	+0.73

TCM5089 276-1301

BLOCK DIAGRAM



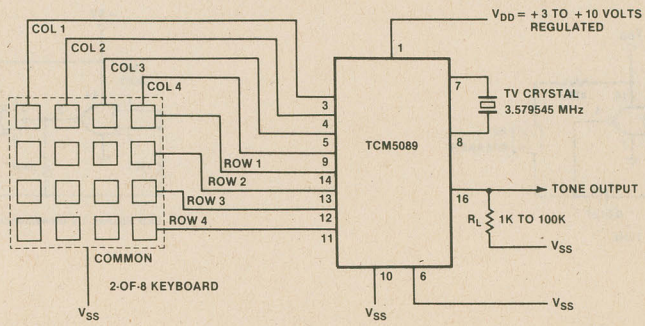
TEST CIRCUITS



Distortion Measurement

Frequency Test

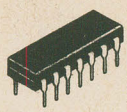
TYPICAL APPLICATION



Typical Hook-up Configuration

4001
276-2401

QUAD TWO-INPUT NOR GATE



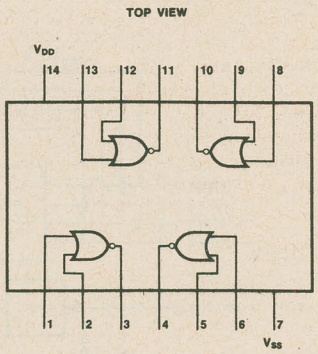
GENERAL DESCRIPTION

The 4001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN CONNECTION



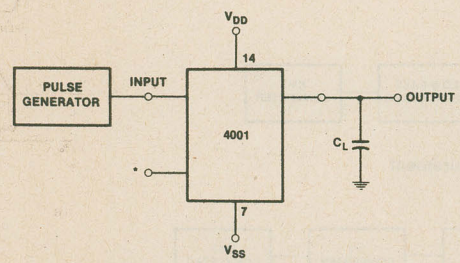
FEATURES

- Quiescent current = 0.5 nA typ/pkg @ 5 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode protection on all inputs
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Single supply operation—positive or negative
- High fanout > 50
- Input impedance = 10^{12} ohms typical
- Logic swing independent of fanout

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

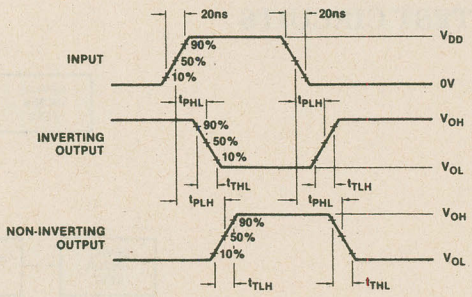
DC Supply Voltage	−0.5 to +16 Vdc
Input Voltage, All Inputs	−0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin	10 mAdc
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C

SWITCH TIME TEST CIRCUIT

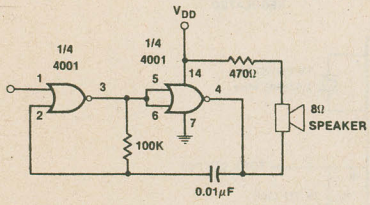


*All unused inputs of OR, NOR gates must be connected to V_{SS}.

SYNC TIMING WAVEFORMS

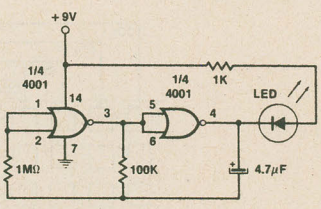


TYPICAL APPLICATIONS



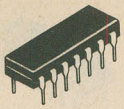
Tone frequency is about 1kHz

Gated Tone Source



LED flashes 1-2 times/second

LED Flasher



QUAD TWO-INPUT NAND GATE

4011
276-2411

GENERAL DESCRIPTION

The 4011 is constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

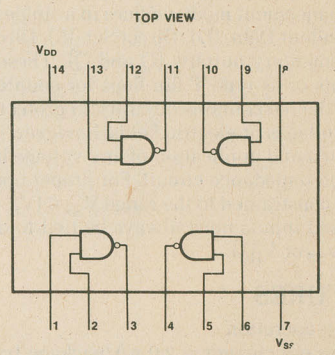
FEATURES

- Quiescent current = 0.5 nA typ/pkg @ 5 Vdc
- Noise immunity = 45% of V_{DD} typical
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Double diode protection on all inputs

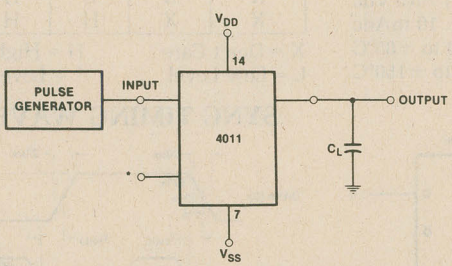
ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

DC Supply ..... −0.5 to +16 Vdc
Input voltage, All Inputs ..... − 0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin ..... 10 mAdc
Operating Temperature Range ..... −40 to +85°C
Storage Temperature Range ..... −65 to +150°C

PIN CONNECTION

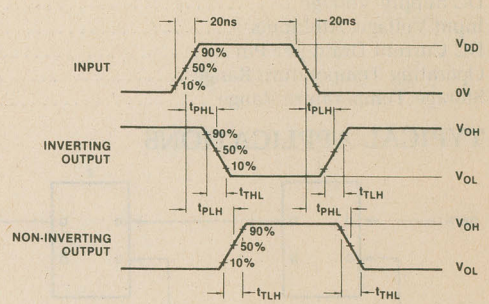


SWITCH TIME TEST CIRCUIT



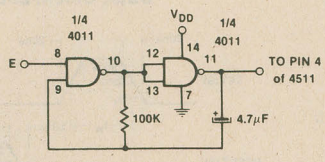
*All unused inputs of AND, NAND gates must be connected to V_{DD}.

SYNC TIMING WAVEFORMS



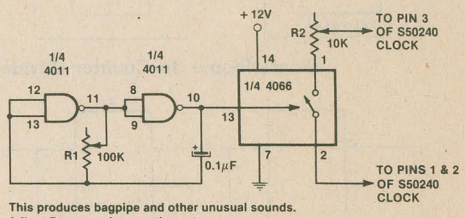
TYPICAL APPLICATIONS

E	DISPLAY
H	FLASHES
L	OFF



Display flashes once per second when E is high.

Display Flasher

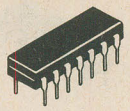


This produces bagpipe and other unusual sounds. Adjust R1 to vary interruption rate.

Special Effects

4013
276-2413

DUAL TYPE D FLIP-FLOP



GENERAL DESCRIPTION

The 4013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

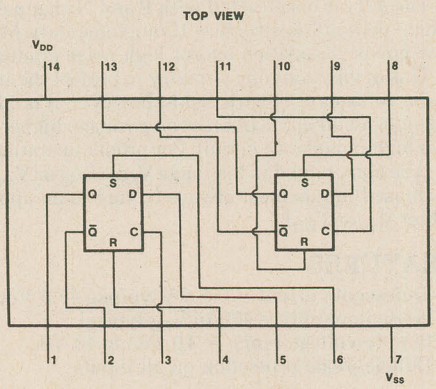
FEATURES

- Static operation
- Quiescent current = 2.0 nA/package typical @ 5 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode protection on all inputs
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Single supply operation
- Toggle rate = 4 MHz typical @ 5 Vdc
- Logic edge-clocked flip-flop design—logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Capable of driving two-low-power TTL loads, one low-power schottky TTL load or two HTL loads over the rated temperature range.

ABSOLUTE MAXIMUM RATINGS
(Voltages referenced to V_{SS})

DC Supply Voltage ..... −0.5 to +16 Vdc
Input Voltage, All Inputs ..... −0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin ..... 10 mAdc
Operating Temperature Range ..... −40 to +85°C
Storage Temperature Range ..... −65 to +150°C

PIN CONNECTION

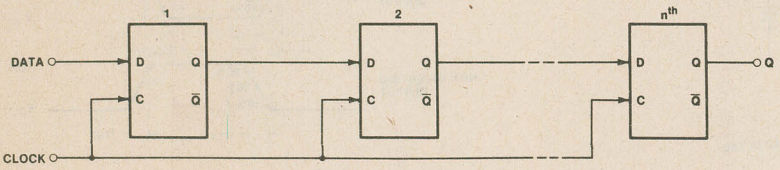


TRUTH TABLE

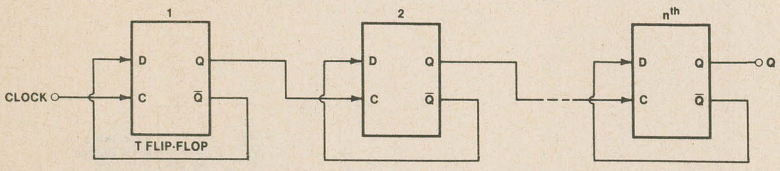
INPUTS				OUTPUTS	
Clock†	Data	Reset	Set	Q	$\overline{Q}$
—	L	L	L	L	H
—	H	L	L	H	L
—	X	L	L	No Change	
X	X	H	L	L	H
X	X	L	H	H	L
X	X	H	H	H	H

X = Don't Care H = High Level
L = Low Level † = Level Change

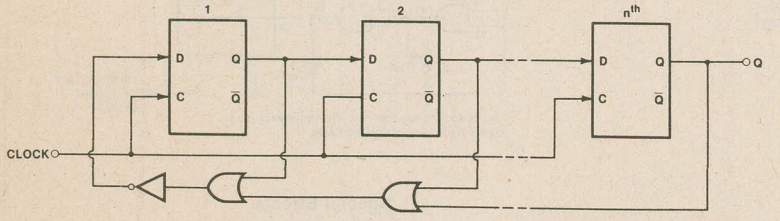
TYPICAL APPLICATIONS



n-Stage Shift Register

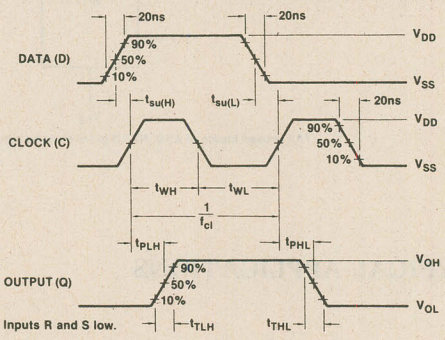


Binary Ripple Up-Counter (Divide-by-2^n)

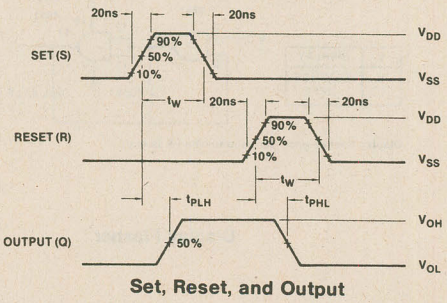


Modified Ring Counter (Divide-by-(n+1))

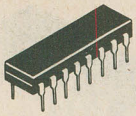
SYNC TIMING WAVEFORMS



Data, Clock, and Output



Set, Reset, and Output



DECADE COUNTER/DIVIDER

4017
276-2417

GENERAL DESCRIPTION

The 4017 is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.

FEATURES

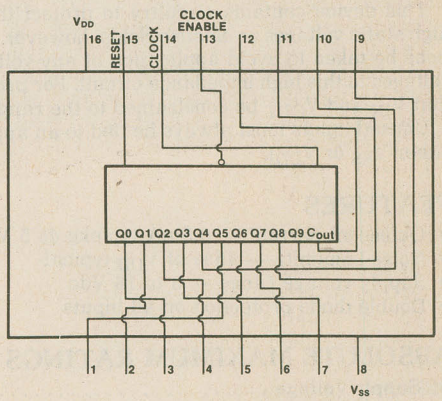
- Fully static operation
- DC clock input circuit allows slow rise times
- Carry out output for cascading
- 12 MHz (typical) operation @ $V_{DD} = 10$ Vdc
- Quiescent current = 5.0 nA/package typical @ 5 Vdc
- Supply voltage range = 3.0 Vdc to 16 Vdc
- Capable of driving two low-power TTL loads, one low-power schottky TTL load or two HTL loads over the rated temperature range

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

DC Supply Voltage	−0.5 to +16 Vdc
Input Voltage, All Inputs	−0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin	10 mAdc
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C

PIN CONNECTION

TOP VIEW

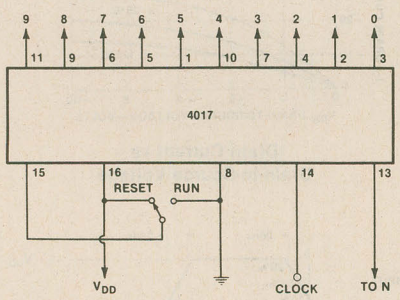


TRUTH TABLE (Positive Logic)

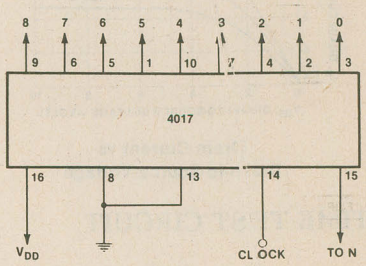
Clock	Clock Enable	Reset	Decode Output = n
L	X	L	n
X	H	L	n
X	X	H	QL
⎍	L	L	n + 1
⎍	X	L	n
X	⎎	L	n
1	⎎	L	n + 1

X = Don't Care If n <5 Carry = "H", Otherwise = "L"
L = Low Level H = High Level

TYPICAL APPLICATIONS



Count to N and Halt

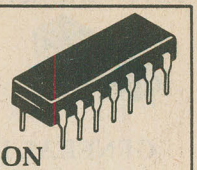


For N = 9, ground pin 15.

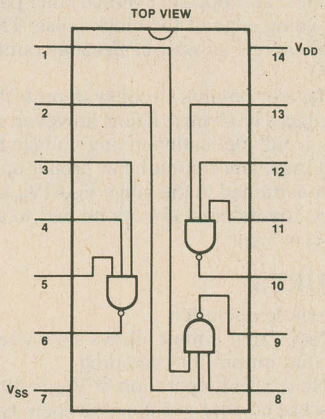
Count to N and Recycle

4023
276-2423

TRIPLE 3-INPUT "NAND" GATE



PIN CONNECTION



GENERAL DESCRIPTION

The 4023 is constructed with P- and N-channel enhancement mode devices in a single monolithic structure. Its primary use is where low power dissipation and/or high noise immunity is desired.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \leqslant (V_{IN}$ or $V_{OUT}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

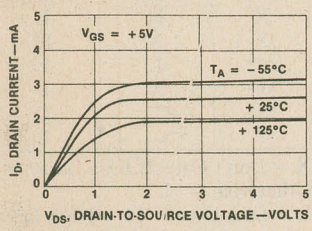
FEATURES

- Quiescent current — 0.5 nA typ/pkg @ 5 Vdc
- Noise immunity — 45% of V_{DD} typical
- Supply voltage range — 3 to 18 Vdc
- Double diode protection on all inputs

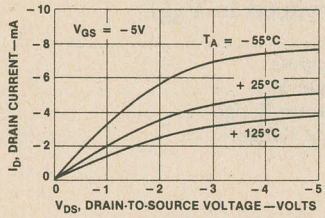
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	−0.5 to +18 V
Input Voltage, All Inputs	−0.5 to +0.5 V
DC Current Drain per Pin	10 mA
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C

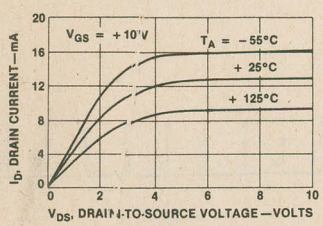
TYPICAL CHARACTERISTICS



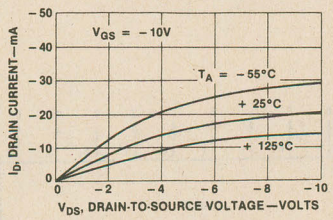
Drain Current vs Drain-to-Source Voltage



Drain Current vs Drain-to-Source Voltage

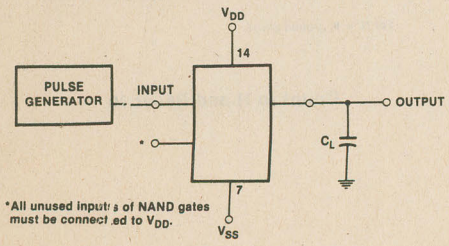


Drain Current vs Drain-to-Source Voltage

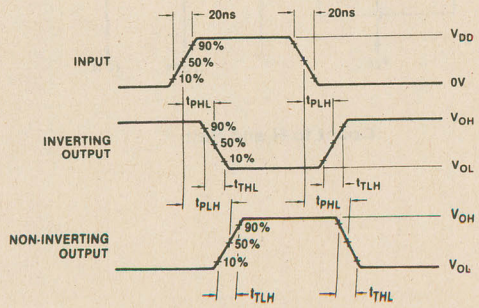


Drain Current vs Drain-to-Source Voltage

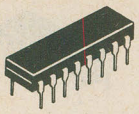
SWITCH TIME TEST CIRCUIT



Test Circuit



Switching Time Waveforms



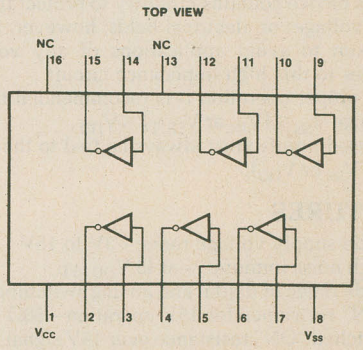
INVERTING HEX BUFFER

4049
276-2449

GENERAL DESCRIPTION

The 4049 hex inverter/buffer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pin 16 is not connected internally on this device; consequently connections to this terminal will not affect circuit operation.

PIN CONNECTIONS



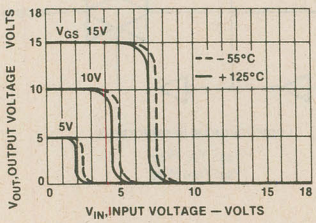
FEATURES

- High source and sink currents
- High-to-low level converter
- Quiescent current = 2.0 nA/package typical @ 5 Vdc
- Supply voltage range = 3.0 Vdc to 16 Vdc

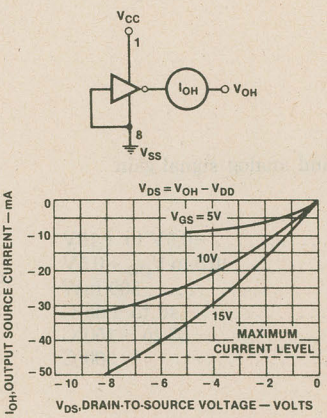
ABSOLUTE MAXIMUM RATINGS
(Voltages referenced to V_{SS}, Pin 8)

DC Supply Voltage ..... −0.5 to +16 Vdc
Input Voltage, All Inputs ..... −0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Input Pin ..... 10 mAdc
DC Current Drain per Output Pin ..... 45 mAdc
Operating Temperature Range ..... −40 to +85°C
Storage Temperature Range ..... −65 to +150°C

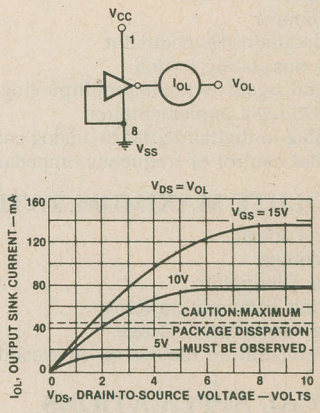
TYPICAL CHARACTERISTICS



Output Voltage vs Input Voltage

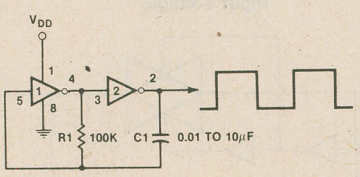


Output Source Current vs Drain-To-Source Voltage



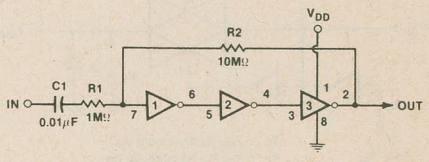
Output Sink Current vs Drain-To-Source Voltage

TYPICAL APPLICATIONS



1,2 = 1/3 4049
Pulse Rate = 1/1.4R1C1

Clock Pulse Generator

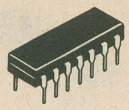


1,2,3 = 1/2 4049
Note that the inverters are used in a LINEAR mode.
Gain = R2/R1

Linear IOX Amplifier

4066
276-2466

QUAD BILATERAL SWITCH



GENERAL DESCRIPTION

The 4066 consists of four independent switches capable of controlling either digital or analog signals. This Quad Bilateral Switch is useful in signal gating, chopper, modulator, demodulator, and CMOS logic implementation.

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$.

Unused inputs must always be tied to the appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FEATURES

- Wide supply voltage range—3V to 15V
- High noise immunity—0.45 V_{DD} typ
- Wide range of digital and analog switching—$\pm$7.5 V_{PEAK}
- "ON" resistance for 15V operation—80Ω typ
- Matched "ON" resistance over 15V signal input—ΔR_{ON} = 5Ω typ
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio—65 dB typ
- High degree of linearity—<0.4% distortion typ
- Extremely low "OFF" switch leakage—0.1 nA typ
- Extremely high control input impedance—$10^{12}\Omega$ typ
- Low crosstalk between switches—−50 dB typ
- Frequency response, switch "ON"—40 MHz typ

APPLICATIONS

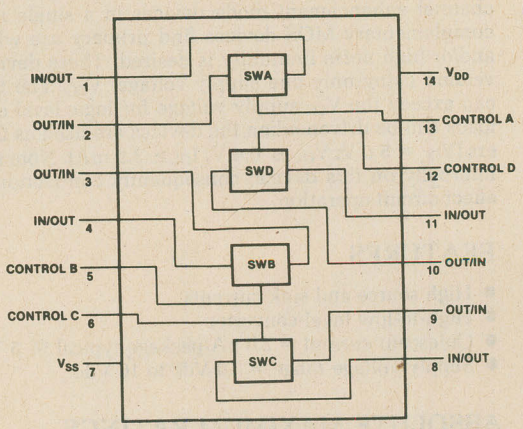
- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.5V to +18V
Input Voltage	−0.5 to V_{DD} +0.5V
Package Dissipation	500 mW
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

PIN CONNECTION

TOP VIEW

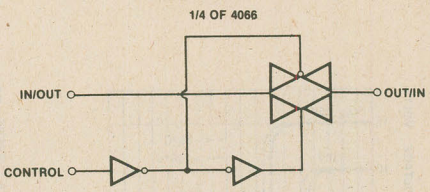


TRUTH TABLES

CONTROL	SWITCH
0	OFF
1	ON

$V_{CONTROL}$	V_{IN} TO V_{OUT} RESISTANCE
V_{SS}	$>10^9$ ohms typical
V_{DD}	3×10^2 ohms typical

LOGIC DIAGRAM

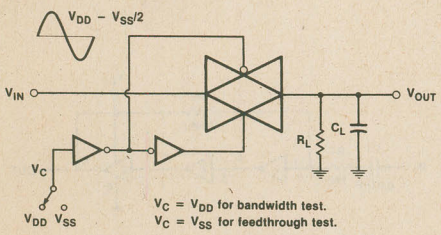


LOGIC DIAGRAM RESTRICTIONS

$V_{SS} < V_{IN} < V_{DD}$

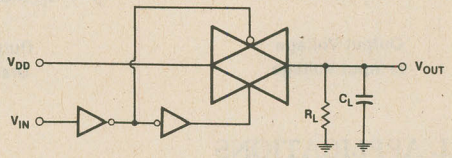
$V_{SS} < V_{OUT} < V_{DD}$

TYPICAL APPLICATIONS

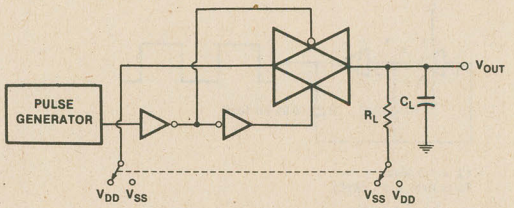


$V_C = V_{DD}$ for bandwidth test.
$V_C = V_{SS}$ for feedthrough test.

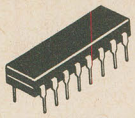
Bandwidth and Feedthrough Attenuation



Input Voltage



Propagation Delay Time, Control to Output



16K DYNAMIC RAM

4116
276-2505

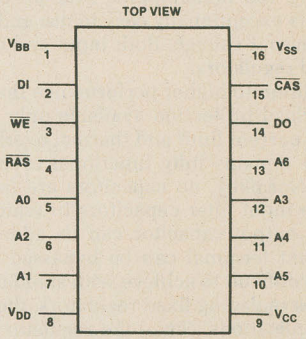
GENERAL DESCRIPTION

The 4116 is a 16,384 × 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the 4116 to be used in page mode operation.

The 4116 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including an RAS-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology is used in the manufacture of the 4116. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the 4116.

PIN CONNECTION



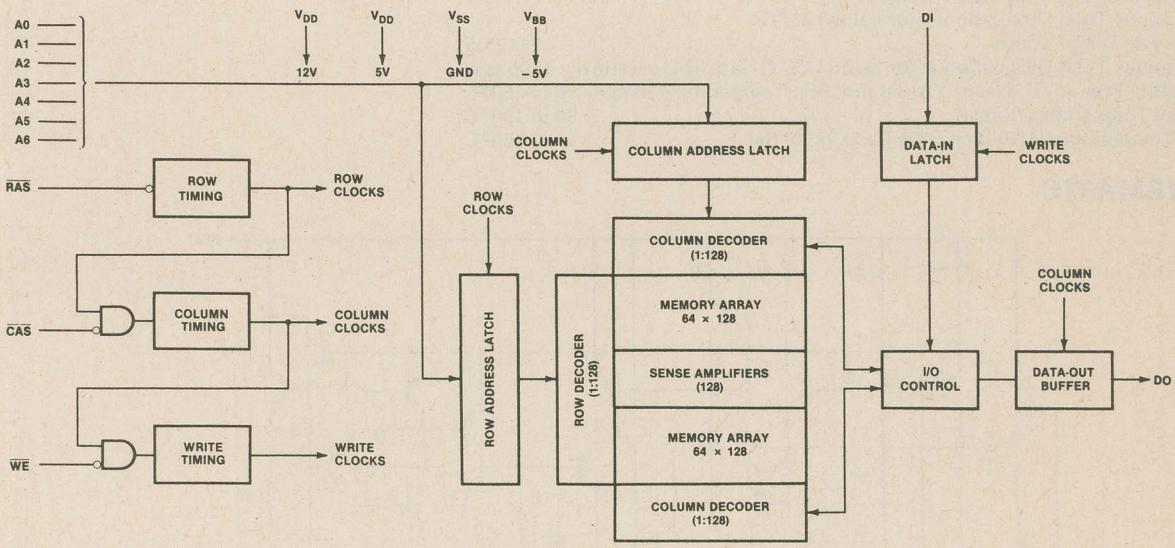
FEATURES

- Access times: 150 ns, 200 ns, 300 ns
- Low power; 462mW max
- TTL compatible: all inputs and output
- Gated CAS—noncritical timing
- Read, wire, read-modify-write and RAS-only refresh cycles
- Page mode operation

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	1W
Supply Voltage V_{DD}	13.2V
Supply Voltage V_{CC}	5.5V
Voltage on Any Pin Relative to V_{BB} ($V_{SS}-V_{BB} \geq 4.5V$)	−0.3 to +20V
Operating Temperature Range	0 to +70°C
Storage Temperature	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

INTERNAL CIRCUIT



Note: All voltages referenced to V_{SS}. When applying voltages to the devices, V_{DD}, V_{CC}, or V_{SS} should never be 0.3V more negative than V_{BB}.

TL317
276-1762

POSITIVE VOLTAGE REGULATOR

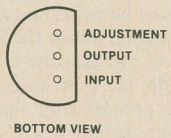
GENERAL DESCRIPTION

The TL317 is an adjustable 3-terminal positive voltage regulator capable of supplying 100 milliamperes over an output-voltage range of 1.2 volts to 32 volts. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Both input and output regulation are better than standard fixed regulators.

In addition to higher performance than fixed regulators, this regulator offers full overload protection available only in integrated circuits. Included on the chip are current limit and thermal overload protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the regulator is useful in a wide variety of other applications. Since the regulator is floating and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. Its primary application is that of a programmable output regulator, but by connecting a fixed resistor between the adjustment terminal and the output terminal, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2 volts where most loads draw little current.

PIN CONNECTION



BOTTOM VIEW

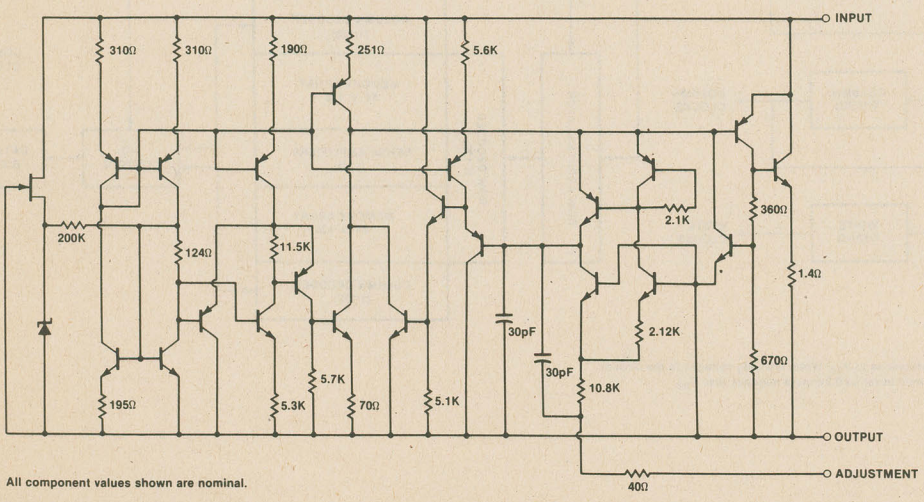
FEATURES

- Output voltage range adjustable from 1.2 V to 32 V
- Guaranteed I_O capability of 100 mA
- Input regulation typically 0.01% per input-volt change
- Output regulation typically 0.5%
- Ripple rejection typically 80 dB

ABSOLUTE MAXIMUM RATINGS

Input-to-Output Differential Voltage, V_I-V_O ..... 35 V
Continuous Total Dissipation at (or below) 25°C
Free-Air Temperature ..... 775 mW
Continuous Total Dissipation at (or below) 25°C Case Temperature .. 1600 mW
Operating Free-Air, Case, or Virtual Junction Temperature Range ..0 to 150°C
Storage Temperature Range ..... −65 to 150°C
Lead Temperature (1/16 inch from Case for 10 Sec.) .....260°C

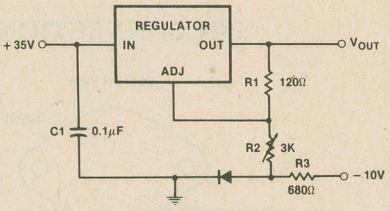
SCHEMATIC



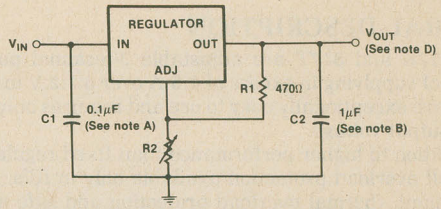
All component values shown are nominal.

TL317 276-1762

TYPICAL APPLICATIONS

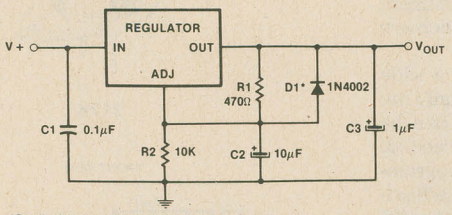


0 to 30 V Regulator Circuit



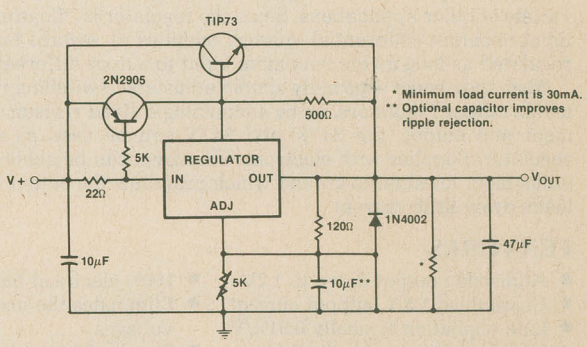
Notes: A. Use of an input bypass capacitor is recommended if regulator is far from filter capacitors.
B. Use of an output capacitor improves transient response but is optional.
C. V_{ref} equals the difference between the output and adjustment terminal voltages.
D. Output voltage is calculated from the equation: $V_{OUT} = V_{ref}(1 + R2/R1)$

Adjustable Voltage Regulator

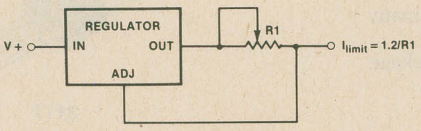


*D1 discharges C2 if output is shunted to ground.

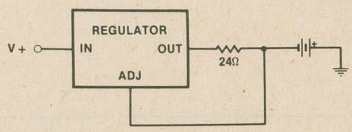
Adjustable Regulator Circuit with Improved Ripple Rejection



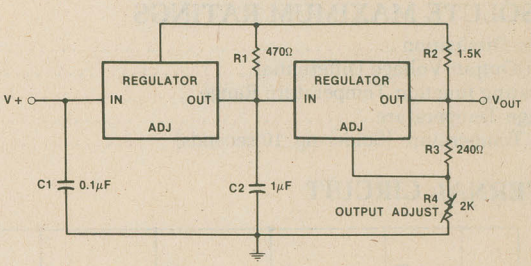
High-Current Adjustable Regulator



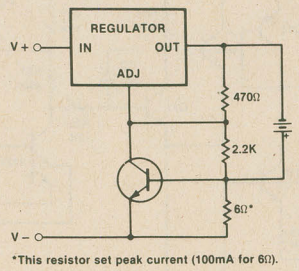
Precision Current Limiter Circuit



50 mA Constant-Current Battery Charger Circuit

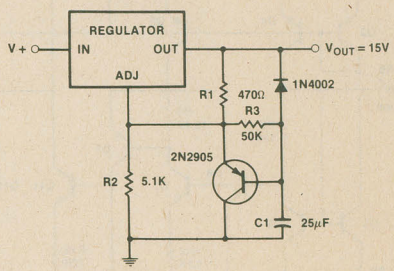


Tracking Preregulator Circuit



*This resistor set peak current (100mA for 6Ω).

Current-Limited 6V Charger



Slow-Turn-On 15 V Regulator Circuit

317K
276-1777
317T
276-1778

3-TERMINAL ADJUSTABLE POSITIVE REGULATOR

GENERAL DESCRIPTION

The 317K and 317T are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over a 1.2 V to 37 V output range. These devices are exceptionally easy to use and requires only two external resistors to set the output voltage.

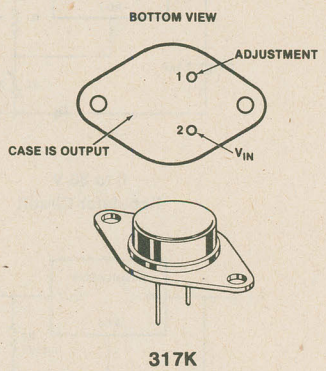
In addition to higher performance than fixed regulators, the 317K and 317T offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the 317K and 317T are useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, they make especially simple adjustable switching regulators, programmable output regulators, or by connecting a fixed resistor between the adjustment and output, the 317K and 317T can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2 V where most loads draw little current.

PIN CONNECTIONS



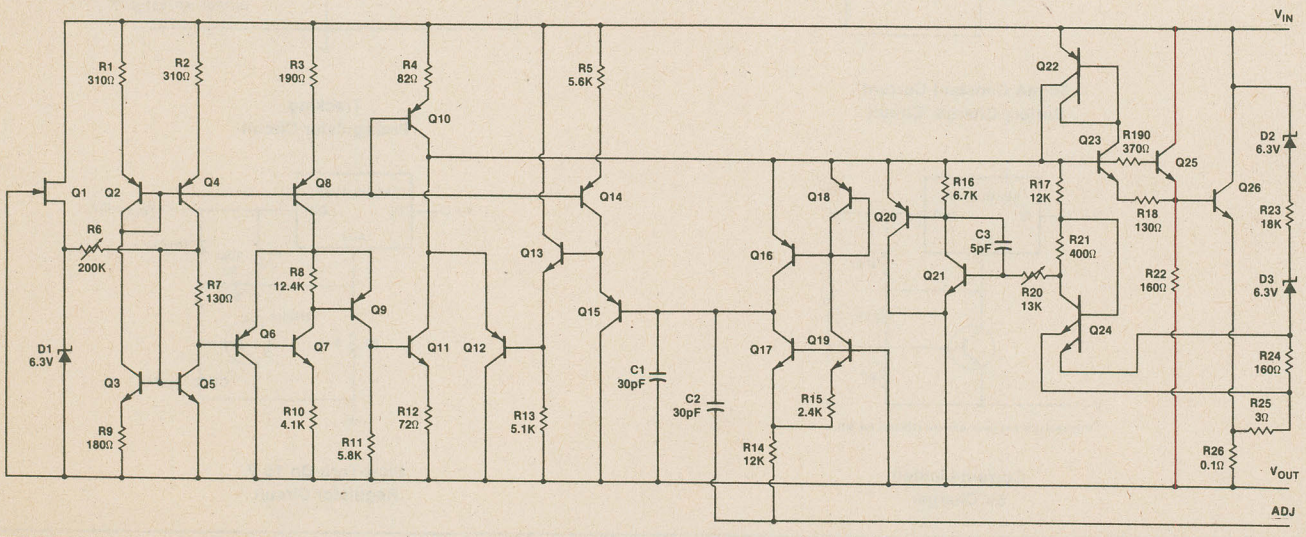
FEATURES

- Adjustable output down to 1.2V
- Guaranteed 1.5A outpput current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

ABSOLUTE MAXIMUM RATINGS

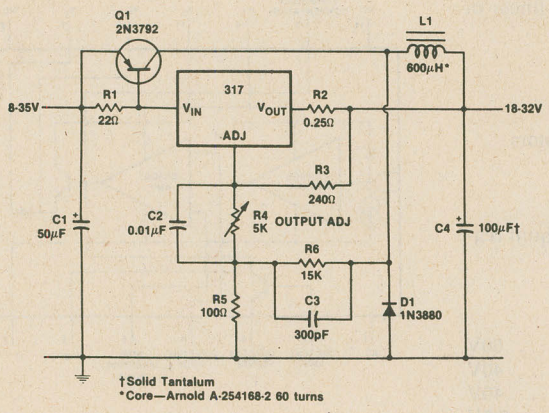
Power Dissipation	Internally limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	0 to +125°C
Storage Temperature	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

INTERNAL CIRCUIT

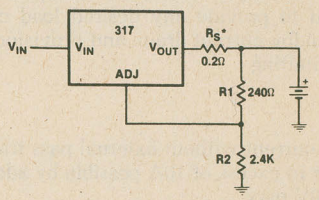


317K 276-1777 317T 276-1778

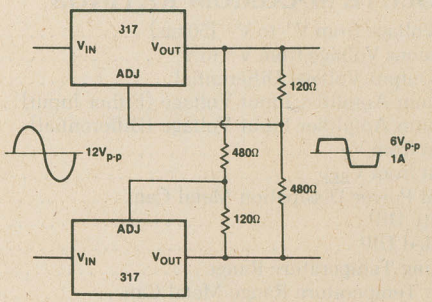
TYPICAL APPLICATIONS



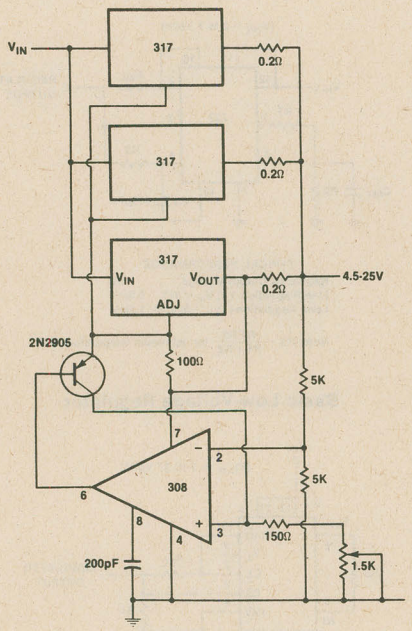
Low Cost 3A Switching Regulator



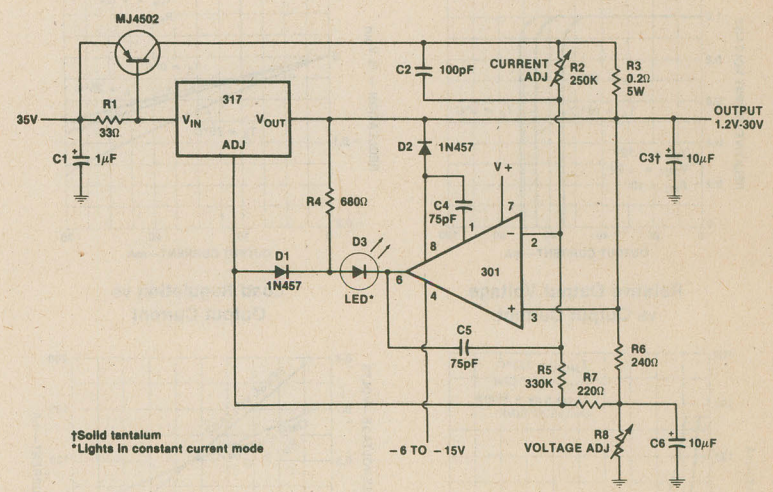
12V Battery Charger



AC Voltage Regulator



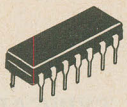
Adjustable 4A Regulator



5A Constant Voltage/Constant Current Regulator

723
276-1740

ADJUSTABLE VOLTAGE REGULATOR



GENERAL DESCRIPTION

The 723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

FEATURES

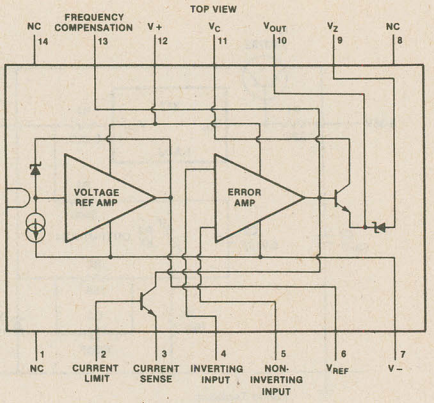
- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

The 723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

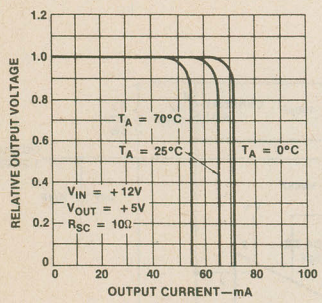
ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V+ to V− (50 ms)	50V
Continuous Voltage from V+ to V−	40V
Input-Output Voltage Differential	40V
Maximum Amplifier Input Voltage (Either Input)	7.5V
Maximum Amplifier Input Voltage (Differential)	5V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation Metal Can	800 mW
Cavity DIP	900 mW
Molded DIP	660 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range Metal Can	−65 to +150°C
DIP	−55 to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

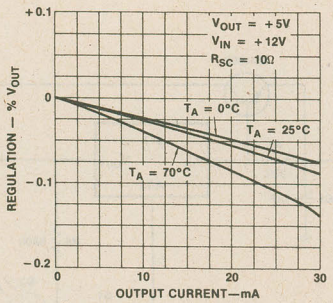
PIN CONNECTION



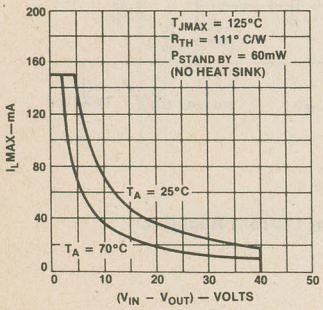
TYPICAL CHARACTERISTICS



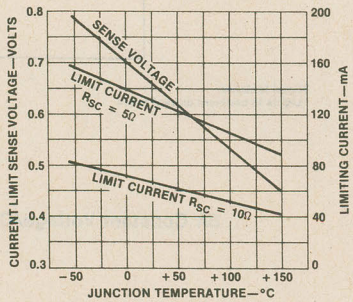
Relative Output Voltage vs Output Current



Load Regulation vs Output Current

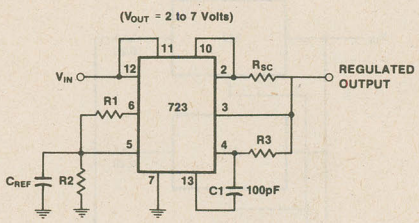


Maximum Load Current vs Input-Output Voltage Differential



Current Limit Sense Voltage vs Junction Temperature

TYPICAL APPLICATIONS

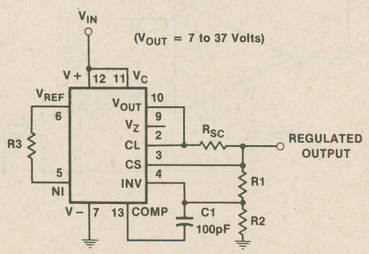


TYPICAL PERFORMANCE

Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 50mA)	1.5mV

Note: R3 = $\frac{R1\ R2}{R1 + R2}$ for minimum temperature drift.

Basic Low Voltage Regulator



TYPICAL PERFORMANCE

Regulated Output Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5mV
Load Regulation (ΔI_L = 50mA)	4.5mV

Note: R3 = $\frac{R1R2}{R1 + R2}$ for minimum temperature drift.

Basic High Voltage Regulator

5V VOLTAGE REGULATOR
12V VOLTAGE REGULATOR
15V VOLTAGE REGULATOR

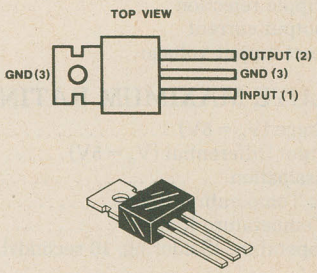
7805 276-1770
7812 276-1771
7815 276-1772

GENERAL DESCRIPTION

This series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

This series will allow over 1.5A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

PIN CONNECTION



FEATURES

- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit

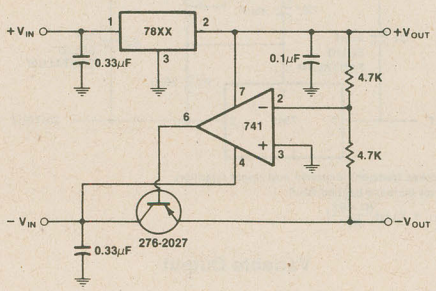
VOLTAGE RANGE

7805	5V
7812	12V
7815	15V

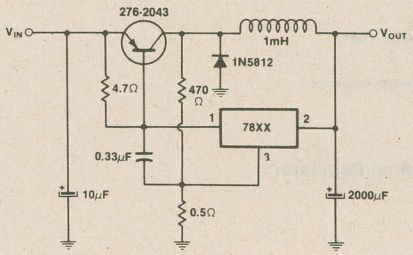
ABSOLUTE MAXIMUM RATINGS

Input Voltage	
(Output Voltage Options 5V through 18V)	35V
(Output Voltage Option 24V)	40V
Internal Power Dissipation	Internally Limited
Maximum Junction Temperature	150°C
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

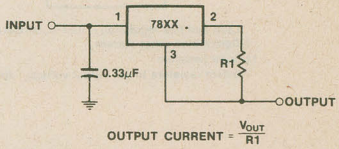
TYPICAL APPLICATIONS



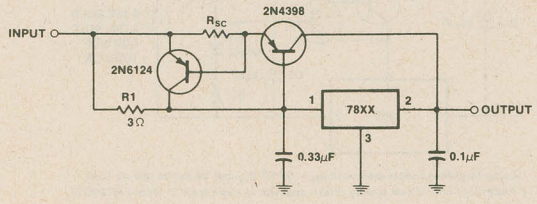
±Tracking Voltage Regulator



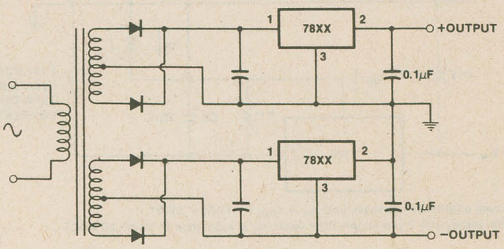
Switching Regulator



Current Regulator



High Output Current, Short Circuit Protected



Positive and Negative Regulator

7905
276-1773

3-TERMINAL NEGATIVE REGULATOR

GENERAL DESCRIPTION

This regulator employs internal current limiting, safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the 7905 allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of this device ensures good regulation in the voltage boosted mode.

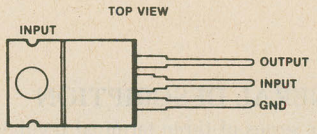
FEATURES

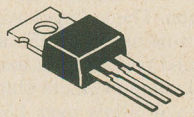
- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% preset output voltage

ABSOLUTE MAXIMUM RATINGS

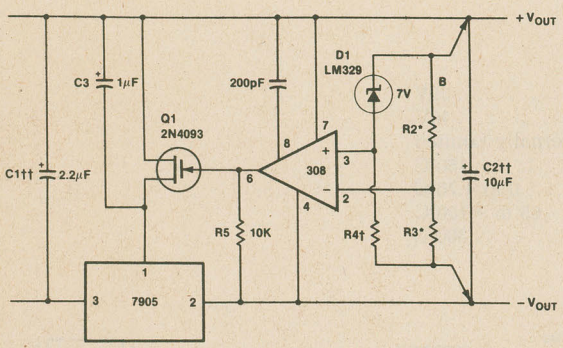
Input Voltage ($V_o = 5V$) ..... −35 V
Input/Output Differential ($V_o = 5V$) ..... 25 V
Power Dissipation ..... Internally Limited
Operating Temperature Range ..... 0 to +125°C
Storage Temperature Range ..... −65 to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 230°C

PIN CONNECTION



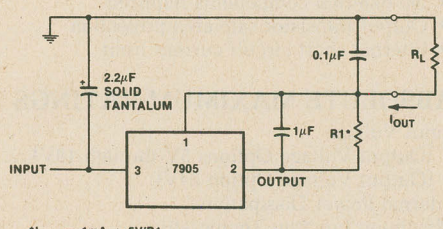


TYPICAL APPLICATIONS



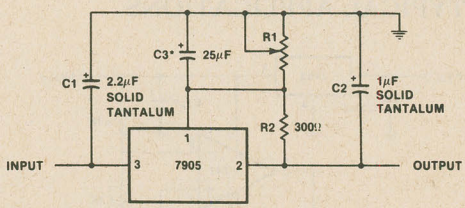
Load and line regulation < 0.01%, temperature stability ≤ 0.2%
† Determines zener current.
†† Solid tantalum
*Select resistors to set output voltage. 2ppm/°C tracking suggested.

High Stability 1 Amp Regulator



*I_{OUT} = 1mA + 5V/R1

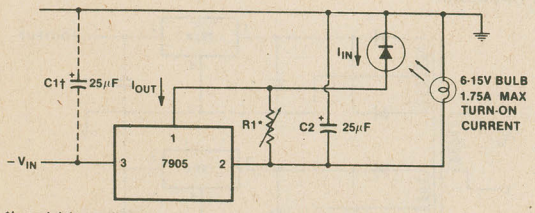
Current Source



*Improves transient response and ripple rejection. Do not increase beyond 50μF.

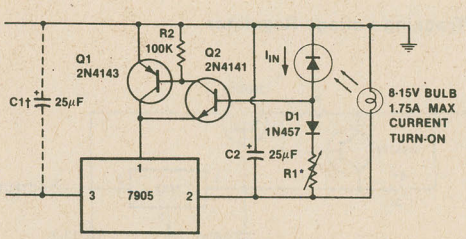
$V_{OUT} = V_{SET}(\frac{R1+R2}{R2})$

Variable Output



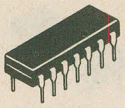
*Lamp brightness increases until $I_{IN} = I_{OUT}$ (≈ 1mA) + 5V/R1.
† Necessary only if raw supply filter capacitor is more than 2" from LM7905CT

Light Controller Using a Silicon Photo Cell



*Lamp brightness increases until I_{IN} = 5V/R1 (I_{IN} can be set as low as 1μA).
† Necessary only if raw supply filter capacitor is more than 2" from LM7905CT.

Light Controller Using a Silicon Photo Cell



QUAD BI-FET OPERATIONAL AMPLIFIER

TL084CN
276-1714

GENERAL DESCRIPTION

The TL084 JFET-input operational amplifier is designed to offer better performance than any previously developed quad-operational amplifier. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

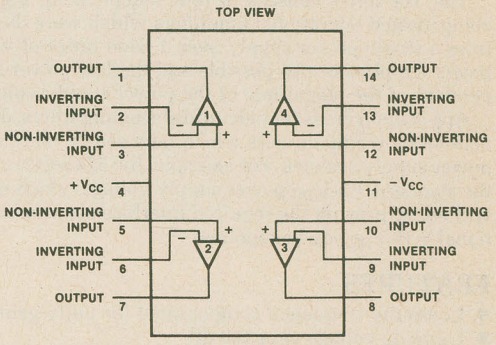
FEATURES

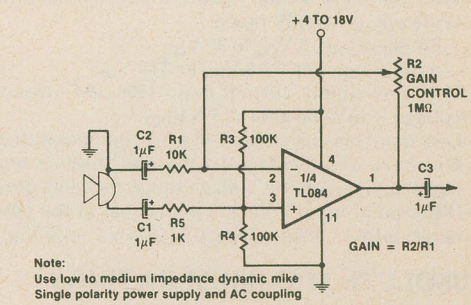
- Low power consumption
- Wide common-mode and differential voltage ranges
- Low input bias and offset currents
- Output short-circuit protection
- High input impedance—JFET-input stage
- Internal frequency compensation
- Latch-up-free operation
- High slew rate—13 V/μs Typ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}+$	18V
Supply Voltage, $V_{CC}-$	−18V
Differential Input Voltage	±30V
Input Voltage	±15V
Duration of Output Short Circuit	Unlimited
Continuous Total Dissipation at (or Below) 25°C Free-Air Temperature	680 mW
Operating Free-Air Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature 1/16 inch from Case for 10 Seconds	260°C

PIN CONNECTION

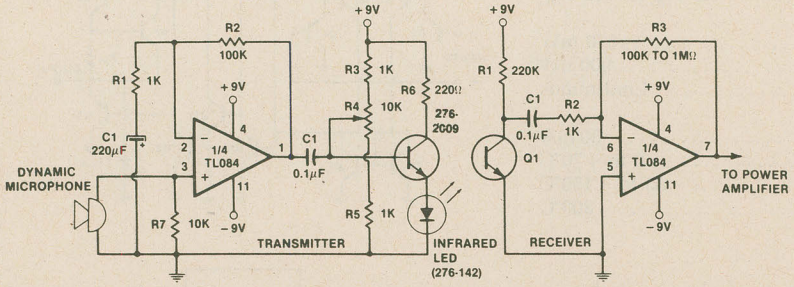




Note:
Use low to medium impedance dynamic mike
Single polarity power supply and AC coupling

Microphone Preamplifier

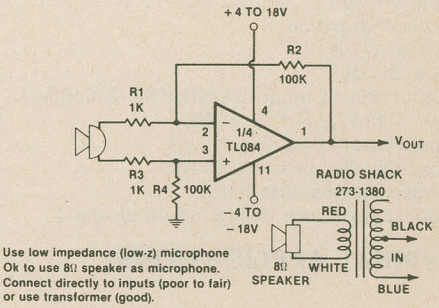
TYPICAL APPLICATIONS



Point the led at Q1 and adjust R4 until best voice quality is obtained. (R4 applies prebias to LED.) R6 limits maximum led current to a safe 40mA.

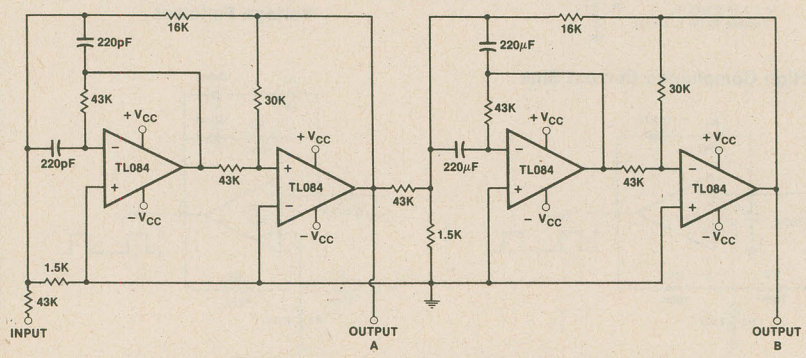
Use RADIO SHACK 276-130 phototransistor for Q1. Maximum range: Hundreds of feet at night with lenses at Q1 and LED.
Power amp: See LM386

Infrared Voice Communicator

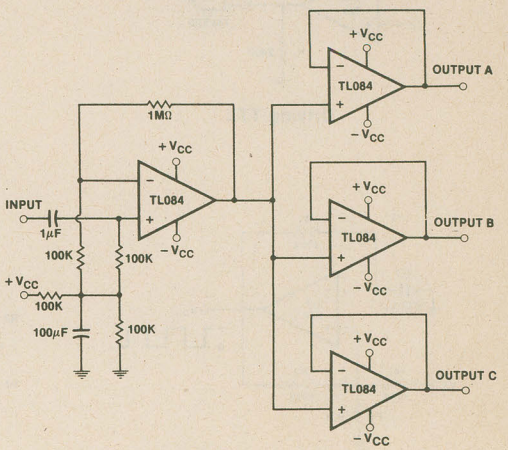


Use low impedance (low-z) microphone
Ok to use 8Ω speaker as microphone.
Connect directly to inputs (poor to fair)
or use transformer (good).

Low-Z Preamplifier



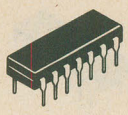
Positive—Feedback Bandpass Filter



Audio Distribution Amplifier

324
276-1711

QUAD OP AMP



GENERAL DESCRIPTION

The 324 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the 324 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional +15 V_{DC} power supplies.

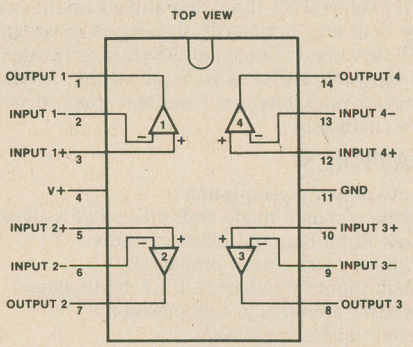
FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  Single supply 3 V_{DC} to 30 V_{DC}
  or dual supplies ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800 μA)—essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC} and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ −1.5 V_{DC}

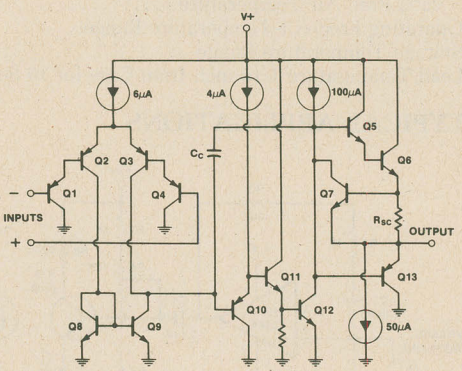
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}
Differential Input Voltage	32 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}
Power Dissipation	
Molded DIP	570 mW
Cavity DIP	900 nW
Output Short-Circuit to GND (One Amplifier)	Continuous
$V^+ \leq 15$ V_{DC} and $T_A = 25°C$	
Input Current ($V_{IN} < -0.3$ V_{OL})	50 mA
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

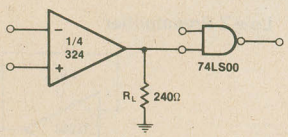
PIN CONNECTION



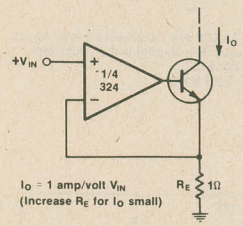
INTERNAL CIRCUIT (Each Amplifier)



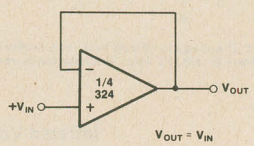
TYPICAL APPLICATIONS



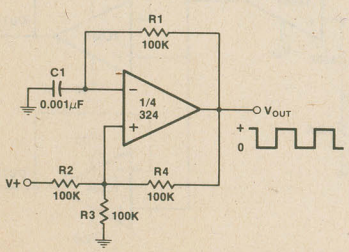
Driving TTL



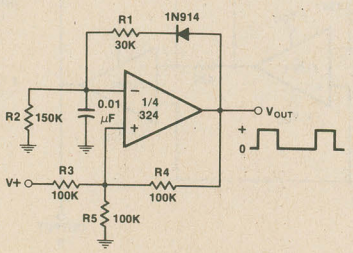
High Compliance Current Sink



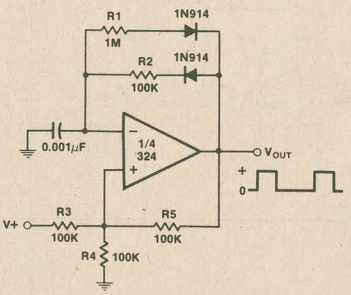
Voltage Follower



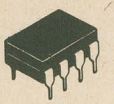
Squarewave Oscillator



Pulse Generator



Pulse Generator



WIDE BANDWIDTH DUAL JFET INPUT OPERATIONAL AMPLIFIER

353
276-1715

GENERAL DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

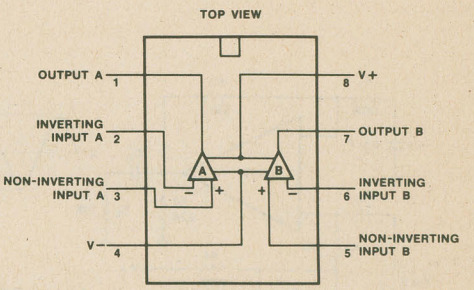
FEATURES

- Internally trimmed offset voltage = 2 mV
- Low input bias current = 50 pA
- Low input noise voltage = 16 nV/√Hz
- Low input noise current = 0.01 pA/√Hz
- Wide gain bandwidth = 4 MHz
- High slew rate = 13 V/μs
- Low supply current = 3.6 mA
- High input impedance = $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz—20kHz = <0.02%
- Low 1/f noise corner = 50 Hz
- Fast settling time to 0.01% = 2 μs

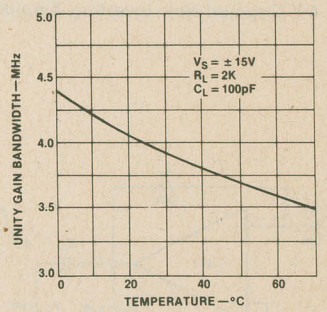
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation	500 mW
Differential Input Voltage	±30V
Input Voltage Range	±15V
Output Short Circuit Duration	Continuous
$T_{j(MAX)}$	115°C
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

PIN CONNECTION

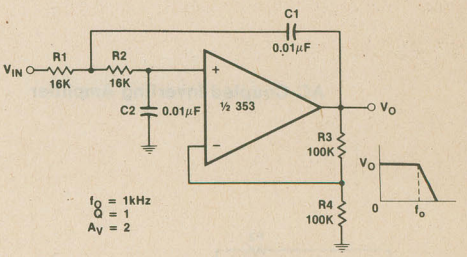


TYPICAL CHARACTERISTICS

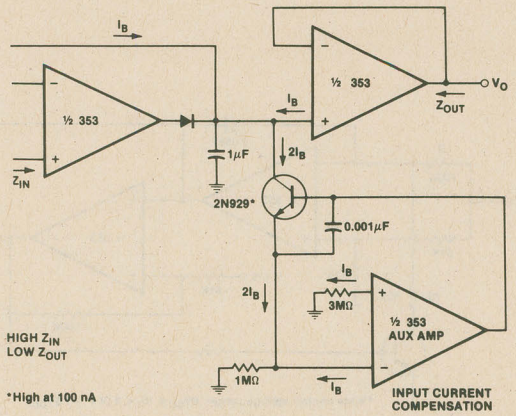


Unity Gain Bandwidth vs Temperature

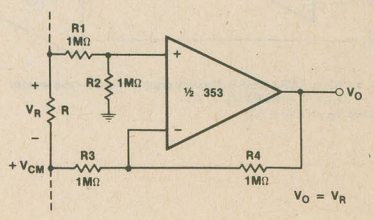
TYPICAL APPLICATIONS



DC Coupled Low-Pass RC Active Filter



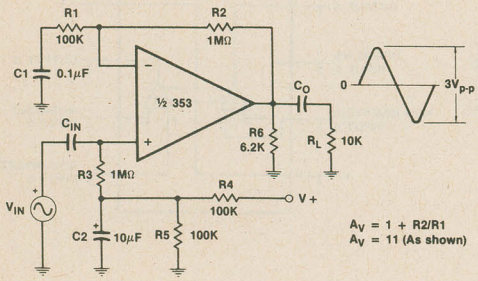
Low Drift Peak Detector



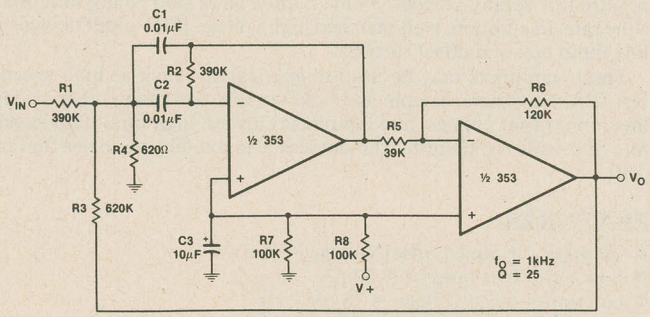
Ground Referencing A Differential Input Signal

353 276-1715

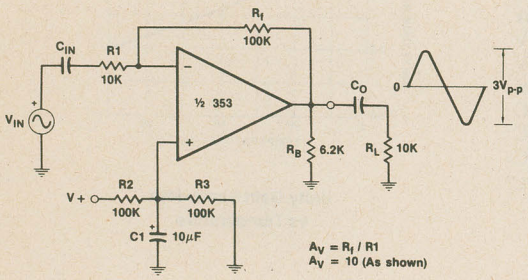
TYPICAL APPLICATIONS (Cont'd)



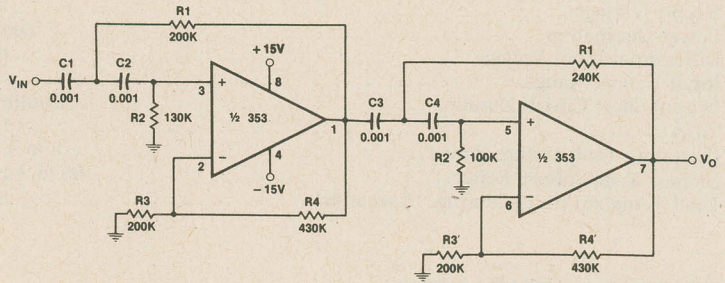
AC Coupled Non-Inverting Amplifier



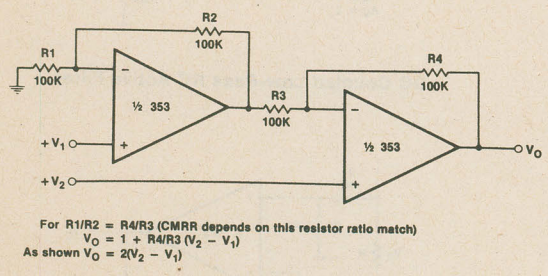
Bandpass Active Filter



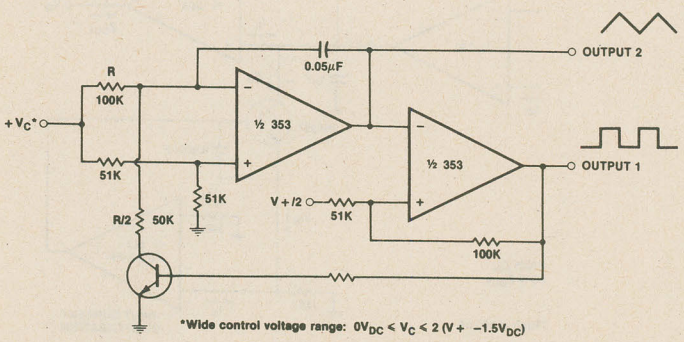
AC Coupled Inverting Amplifier



Fourth Order High Pass Butterworth Filter



High Input Z, DC Differential Amplifier



Voltage Controlled Oscillator (VCO)

OPERATIONAL AMPLIFIER

741
276-007

GENERAL DESCRIPTION

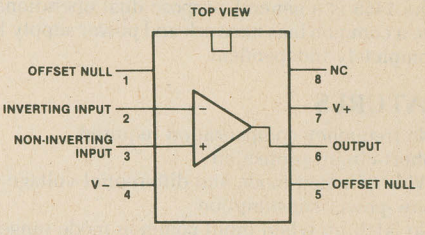
The 741 series are general purpose operational amplifiers which feature improved performance over industry standards.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

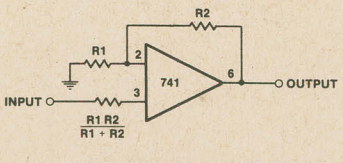
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±16V
Power Dissipation ..... 500 mW
Differential Input Voltage ..... ±30V
Input Voltage ..... ±15V
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0 to +70°C
Storage Temperature Range ..... −65 to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

PIN CONNECTION

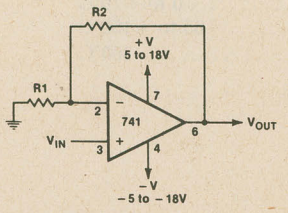


TYPICAL APPLICATIONS



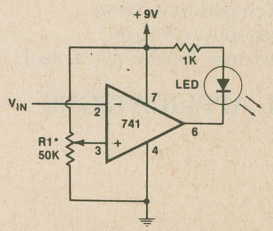
GAIN	R1	R2	BW	R_{IN}
10	1K	9K	100kHz	400MΩ
100	100Ω	9.9K	10kHz	280MΩ
1000	100Ω	99.9K	1kHz	80MΩ

Non-Inverting Amplifier



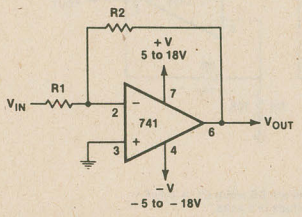
$V_{OUT} = V_{IN} (1 + R2/R1)$

Non-Inverting Amplifier



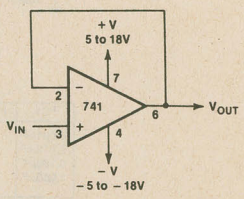
*R1 sets the voltage detection threshold (up to +9V).
When V_{IN} exceeds the threshold (reference), the LED glows.

Level Detector



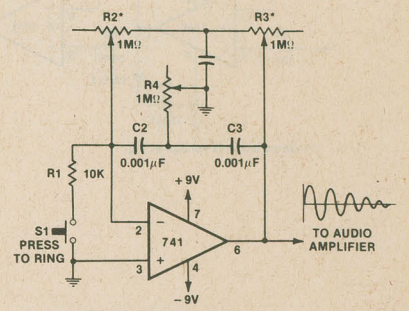
$V_{OUT} = -V_{IN} (R2/R1)$

Inverting Amplifier



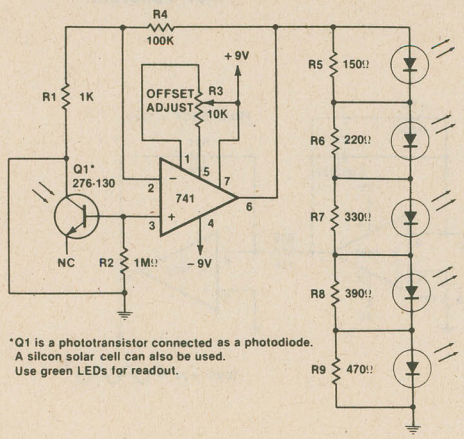
$V_{OUT} = V_{IN}$

Unity Gain Follower



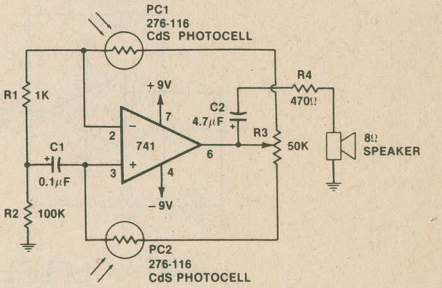
*Adjust R3 to just below oscillation point.
Adjust R2 and R3 for sounds such as bell, drum, tinkling, etc.

Electronic Bell



*Q1 is a phototransistor connected as a photodiode.
A silicon solar cell can also be used.
Use green LEDs for readout.

Bargraph Light Meter



Light on PC1 decreases tone frequency
Light on PC2 increases tone frequency

Audible Light Sensor

1458
276-038

DUAL OPERATIONAL AMPLIFIER

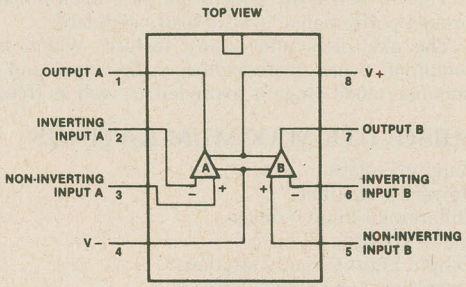
GENERAL DESCRIPTION

The 1458 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

FEATURES

- No frequency compensation required.
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- No latch up when input common mode range is exceeded

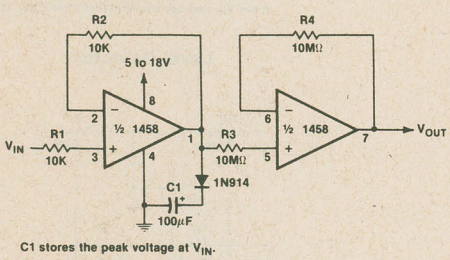
PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

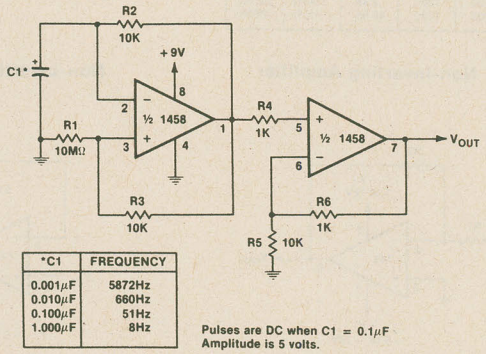
Supply Voltage	±16V
Power Dissipation	400 mW
Differential Input Voltage	±30V
Input Voltage	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

TYPICAL APPLICATIONS



C1 stores the peak voltage at V_{IN}.

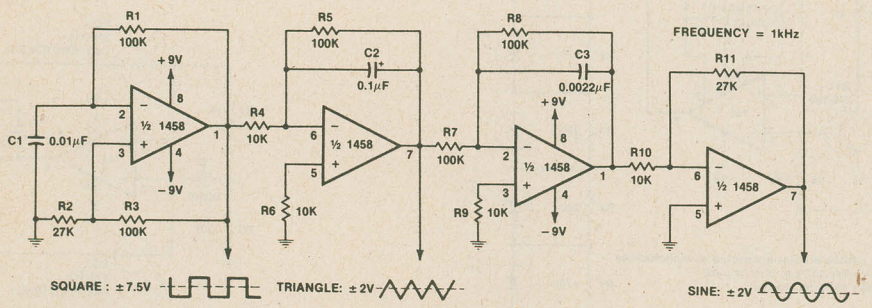
Peak Detector



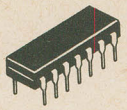
*C1	FREQUENCY
0.001μF	5872Hz
0.010μF	660Hz
0.100μF	51Hz
1.000μF	8Hz

Pulses are DC when C1 = 0.1μF
Amplitude is 5 volts.

Pulse Generator



Function Generator



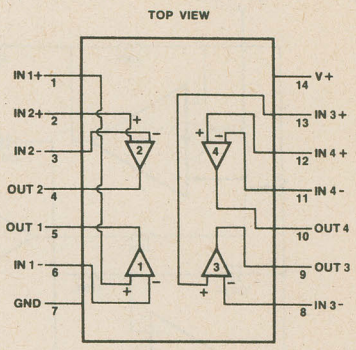
QUAD OPERATIONAL NORTON AMPLIFIER

3900
276-1713

GENERAL DESCRIPTION

The 3900 series consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: ac amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

PIN CONNECTION



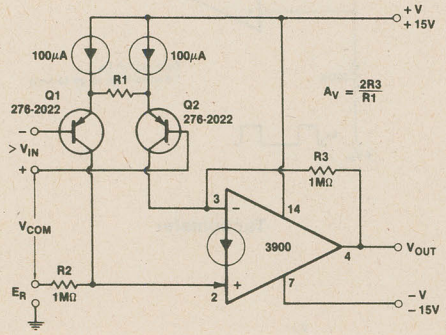
FEATURES

- Wide single supply voltage 4 V_{DC} to 36 V_{DC} range or dual supplies ± 2 V_{DC} to ± 18 V_{DC}
- Supply current drain independent of supply voltage
- Low input biasing current 30 nA
- High open-loop gain 70 dB
- Wide bandwidth 2.5 MHz (Unity Gain)
- Large output voltage swing $(V^+ - 1)$ $V_{p\text{-}p}$
- Internally frequency compensated for unity gain
- Output short-circuit protection

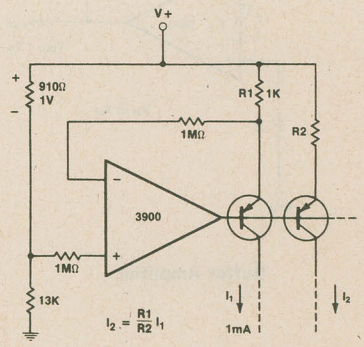
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Wide Range, Single Supply) . . . . . 32 V_{DC}
Supply Voltage (Wide Range, Dual Supply) . . . . . ± 16 V_{DC}
Power Dissipation ($T_A = 25°C$)
Flat Pack . . . . . 570 mW
Input Currents, I_{IN}^+ or I_{IN}^- . . . . . 20 mA_{DC}
Output Short-Circuit Duration—One Amplifier . . . . . Continuous
$T_A = 25°C$ (See Application Hints)
Operating Temperature Range . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

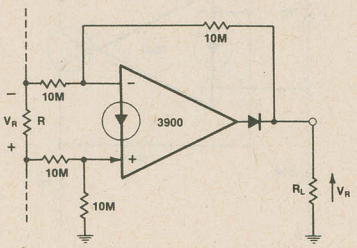
TYPICAL APPLICATIONS



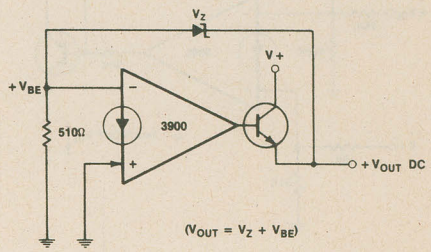
Basic Instrumentation Amplifier



Fixed Current Sources



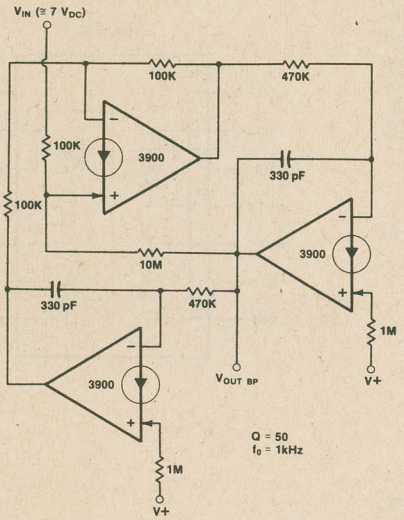
Ground-Referencing a Differential Input Signal



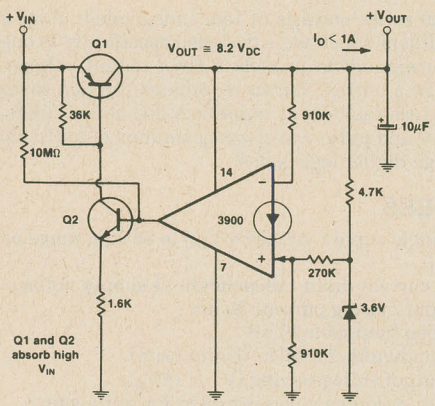
Voltage Regulator

3900 276-1713

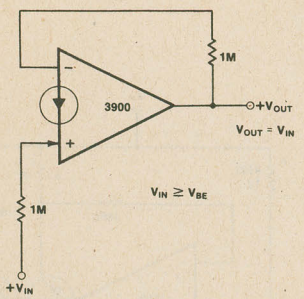
TYPICAL APPLICATIONS (Con't)



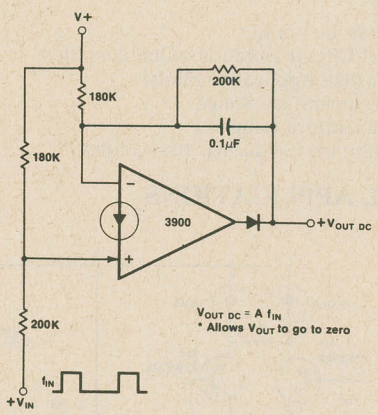
Bi-Quad Active Filter
(2nd Degree State-Variable Network)



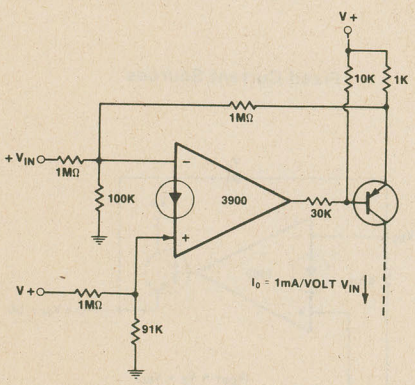
High V_{IN}, Low (V_{IN} − V_{OUT}) Self Regulator



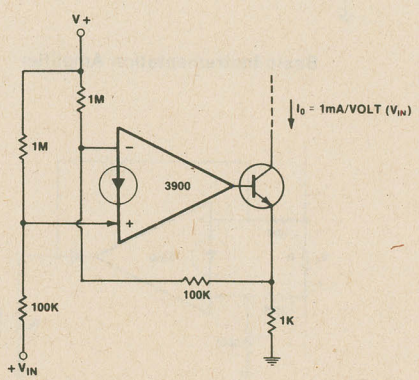
Buffer Amplifier



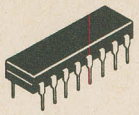
Tachometer



Voltage Controlled Current Source
(Transconductance Amplifier)



Voltage-Controlled Current Sink
(Transconductance Amplifier)



PROGRAMMABLE TIMER/COUNTER

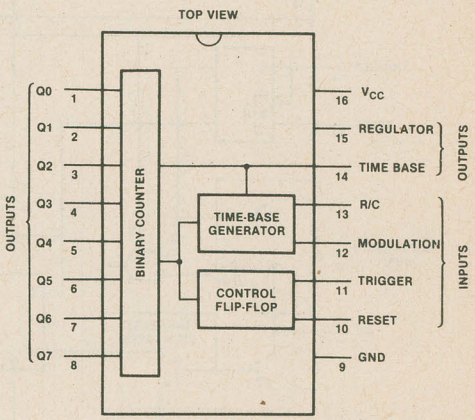
uA2240C
276-1735

GENERAL DESCRIPTION

These circuits consist of a time-base oscillator, an eight-bit counter, a control flip-flop, and a voltage regulator. The frequency of the time-base oscillator is set by the time constant of an external resistor and capacitor at pin 13 and can be synchronized or modulated by signals applied to the modulation input. The output of the time-base section is applied directly to the input of the counter section and also appears at pin 14 (time base). The time-base pin may be used to monitor the frequency of the oscillator, to provide an output pulse to other circuitry, or (with the time-base section disabled) to drive the counter input from an external source. The counter input is activated on a negative-going transition. The reset input stops the time-base oscillator and sets each binary output, Q0 through Q7, and the time-base output to a TTL high level. After resetting, the trigger input starts the oscillator and all Q outputs go low. Once triggered, the uA2240 will ignore any signals at the trigger input until it is reset.

This timer/counter may be operated in the free-running mode or with output-signal feedback to the reset input for automatic reset. Two or more binary outputs may be connected together to generate complex pulse patterns, or each output may be used separately to provide eight output frequencies. Using two circuits in cascade can provide precise time delays of up to three years.

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... 18 V
Output Voltage: Q0 thru Q7 ..... 18 V
Output Current: Q0 thru Q7 ..... 10 mA
Regulator Output Current ..... −5 mA
Continuous Dissipation at (or below) 25°C Free-Air Temperature ..... 650 mW
Operating Free-Air Temperature Range ..... 0 to 70°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage ..... 15 V
Timing Resistor ..... 10 MΩ
Timing Capacitor ..... 1000 μF
Counter Input Frequency (Pin 14) ..... 1.5 MHz
Pull-Up Resistor, Time-Base Output ..... 20 KΩ
Trigger and Reset Input Pulse Voltage ..... 2 to 3 V
Trigger and Reset Input Pulse Width ..... 2 μs
External Clock Input Pulse Voltage ..... 3 V
External Clock Input Pulse Width ..... 1 μs

TEST CIRCUITS

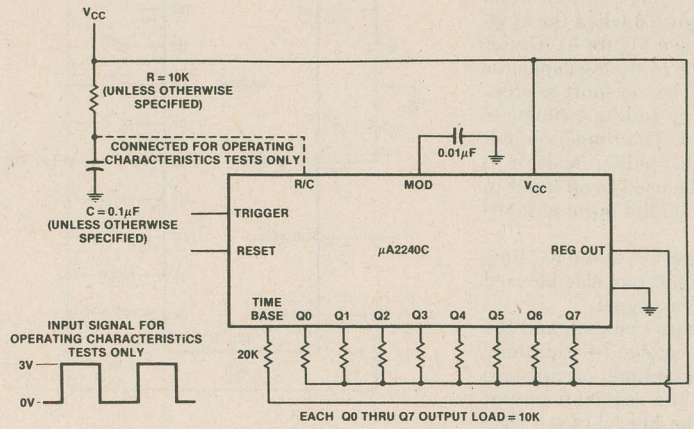


Figure 1—General Test Circuit

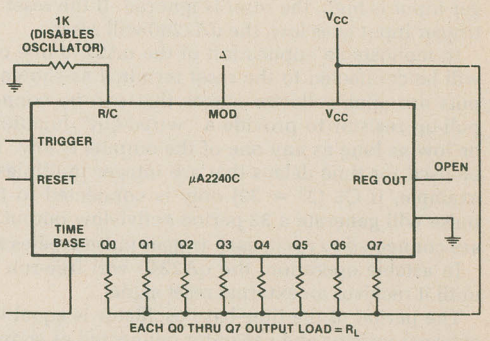


Figure 2—Counter Test Circuit

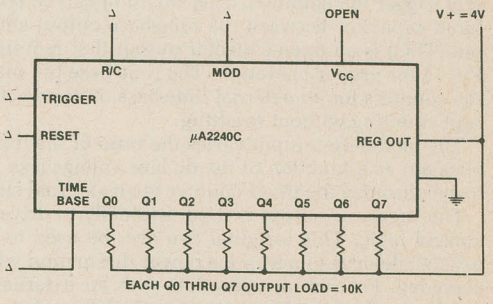
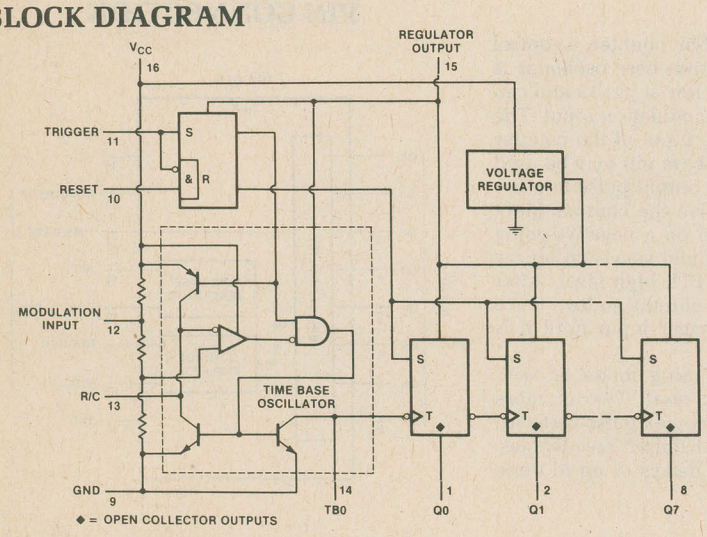


Figure 3—Reduced-Power Test Circuit (Time Base Disabled)

uA2240C 276-1735

BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

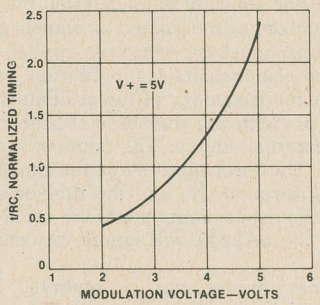


Figure 4—
Normalized Time-Base Period
Modulation Input Voltage

TYPICAL APPLICATIONS

These are voltage waveforms for typical operation of the uA2240. If both reset and trigger inputs are low during power-up, the timer/counter will be in a reset state with all binary (Q) outputs high and the oscillator stopped. In this state, a high level on the trigger input starts the time-base oscillator. The initial negative-going pulse from the oscillator sets the Q outputs to low logic levels at the beginning of the first time-base period. The uA2240 will ignore any further signals at the trigger input until after a reset signal is applied to the reset input. With the trigger input low, a high level at the reset input will set Q outputs high and stop the time-base oscillator. If the reset signal occurs while the trigger input is high, the reset is ignored. If the reset input remains high when the trigger input goes low, the uA2240 will reset.

In monostable application of the uA2240 one or more of the binary outputs will be connected to the reset terminal as shown in Figure 6. The binary outputs are open-collector stages that can be connected together to a common pull-up resistor to provide a "wired-OR" function. The combined output will be low as long as any one of the outputs is low. This type of arrangement can be used for time delays that are integer multiples of the time-base period. For example, if Q5 ($2^5 = 32$) only is connected to the reset input, every trigger pulse will generate a 32-period active-low output. Similarly, if Q0, Q4, and Q5 are connected to reset, each trigger pulse creates a 49-period delay.

In astable operation, the uA2240 will free-run from the time it is triggered until it receives an external reset signal.

The period of the time-base oscillator is equal to the RC time constant of an external resistor and capacitor connected as shown in Figure 6 when the modulation input is open (approximately 3.5 volts internal, see Figure 4). Under conditions of high supply voltage ($V_{CC} > 7$ V) and low value of timing capacitor ($C < 0.1\mu F$), the pulse width of the time-base oscillator may be too short to properly trigger the counters. This situation can be corrected by adding a 300-picofarad capacitor between the time-base output and ground. The time-base output (TBO) is an open-collector output that requires a 20-KΩ pull-up resistor to Pin 15 for proper operation. The time-base pin may also be used as an input to the counters for an external time-base or as an active-low inhibit input to interrupt counting without resetting.

The modulation input varies the ratio of the time-base period to the RC time constant as a function of the dc bias voltage (see Figure 4). It can also be used to synchronize the timer/counter to an external clock or sync signal.

The regulator output is used internally to drive the binary counters and the control logic. This terminal can also be used to supply voltage to additional uA2240 devices to minimize power dissipation when several timer circuits are cascaded. For circuit operation with an external clock, the regulator output can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 volts are used with the internal time base, pin 15 should be shorted to pin 16.

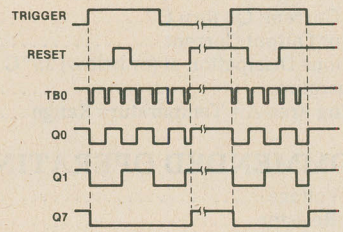


Figure 5—Timing Diagram
of Output Waveforms

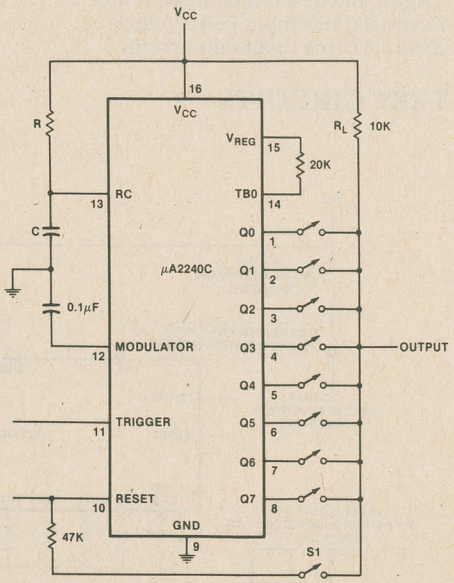
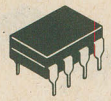


Figure 6—Basic Connections
for Timing Applications

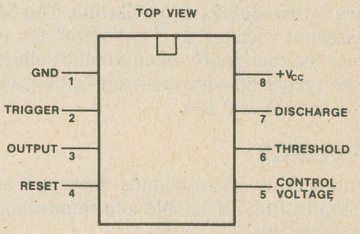


TIMER 555
276-1723

GENERAL DESCRIPTION

The 555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

PIN CONNECTION



FEATURES

- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

ABSOLUTE MAXIMUM RATINGS

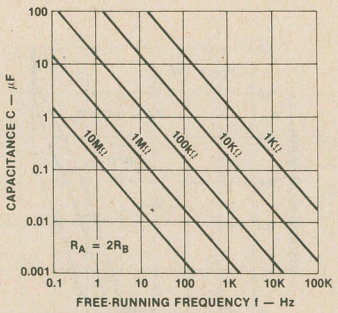
Supply Voltage	+16V
Power Dissipation	600 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TRUTH TABLE

PIN 2 TRIGGER	PIN 6 THRESHOLD	PIN 4 RESET	PIN 3 OUTPUT
H	X	H	L
L	X	H	H
H	L	H	L
X	X	L	L

X = Don't Care L = Low Level H = High Level

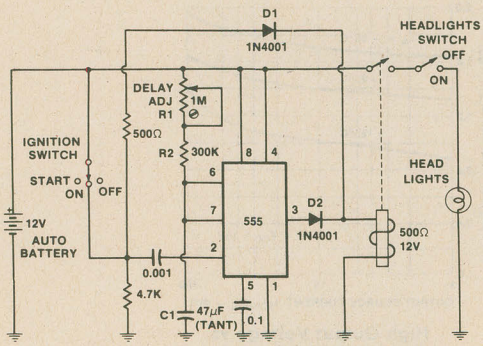
TYPICAL CHARACTERISTICS



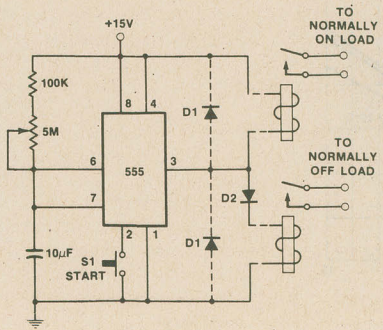
Capacitance vs Free-Running Frequency

The charge time (output high) is given by: $t_1 = 0.693 (R_A + R_B) C$
The discharge time (output low) is given by: $t_2 = 0.693 (R_B) C$
Thus the total period is: $T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$
The frequency of oscillation is: $f = 1/T = 1.44 / (R_A + 2R_B) C$

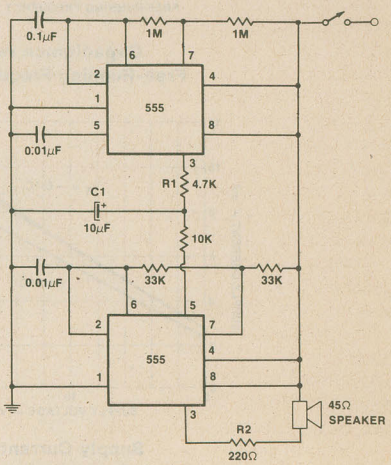
TYPICAL APPLICATIONS



Automatic Headlight Turn-Off Circuit



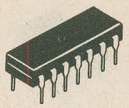
Relay Timer



Warble Alarm Circuit

556
276-1728

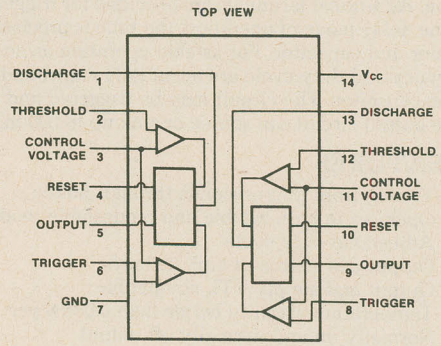
DUAL TIMER



GENERAL DESCRIPTION

The 556 dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

PIN CONNECTION



FEATURES

- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

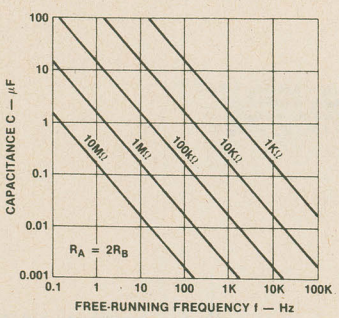
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

ABSOLUTE MAXIMUM RATINGS

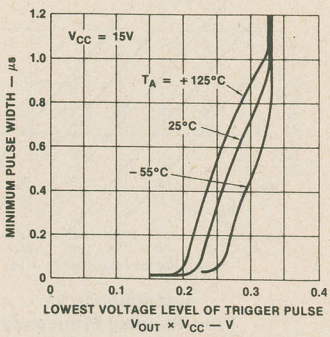
Supply Voltage	+16V
Power Dissipation	600 mW
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL CHARACTERISTICS

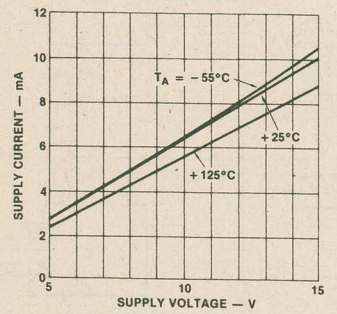


Capacitance vs Free-Running Frequency

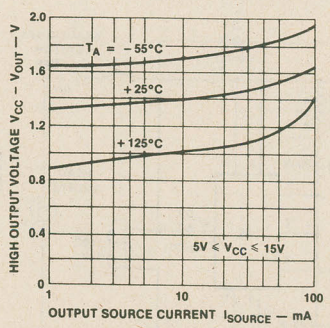
The charge time (output high) is given by:
$t_1 = 0.693 (R_A + R_B) C$
The discharge time (output low) is given by:
$t_2 = 0.693 (R_B) C$
Thus the total period is:
$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$
The frequency of oscillation is:
$f = 1/T = 1.44 / (R_A + 2R_B) C$



Minimum Pulse Width vs Lowest Voltage Level of Trigger Pulse



Supply Current vs Supply Voltage



High Output Voltage vs Output Source Current

LOW POWER GENERAL PURPOSE TIMER

7555
276-1743

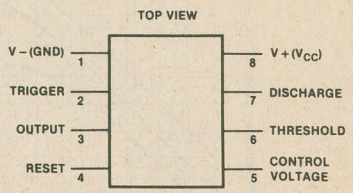
GENERAL DESCRIPTION

The 7555 is a CMOS RC timer providing significantly improved performance over standard timers. Improved parameters include the low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER and RESET currents, no crowbarring of the supply current during any output transition, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the 7555 is a stable controller capable of producing accurate time delays or frequency. In the time delay one shot mode of operation for each circuit, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor.

The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink large currents to drive TTL loads or provide minimal offsets to drive CMOS loads.

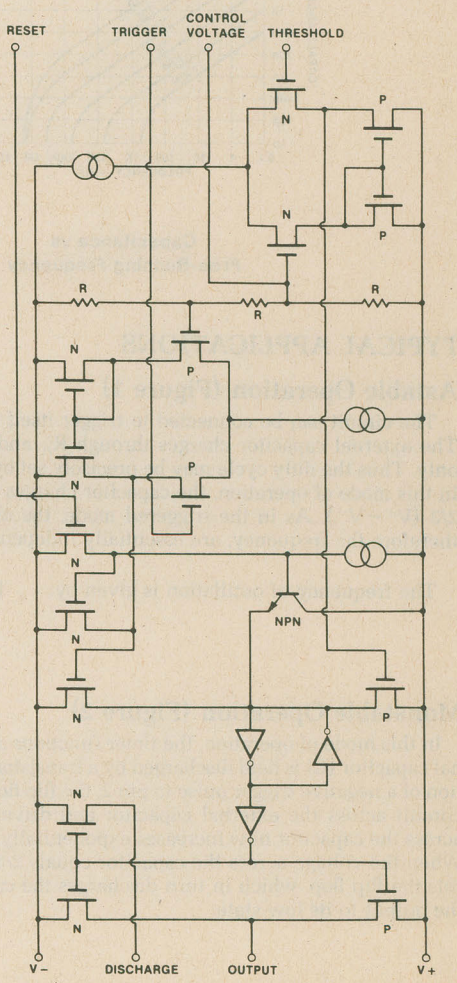
PIN CONNECTION



FEATURES

- Low Supply Current—80μA typical
- Extremely low trigger, threshold and reset currents—20pA typical
- High speed operation—500 kHz guaranteed
- Wide operation supply voltage range guaranteed 2 to 18 volts
- Well behaved reset function—no crowbarring of supply during output transition.
- Can be used with higher impedance timing elements than regular 555 for longer RC time constants.
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver-can drive TTL/CMOS
- Typical temperature stability of 0.005% per °C at 25°C
- Normally on and normally off output with very low offsets
- Completely static protected—no special handling considerations.

INTERNAL CIRCUIT



APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V^+ - V^-$ ..... +18V
Input Voltage, Trigger, Threshold, Reset,
Control Voltage (see note) ..... $\leq V^+ + 0.3V$ to $\geq V^- - 0.3V$
Output Current ..... 100 mA
Power Dissipation ..... 200 mW
Operating Temperature Range ..... −20 to +70°C
Storage Temperature Range ..... −65 to +150°C
Lead Temperature (Soldering, 60 Seconds) ..... +300°C

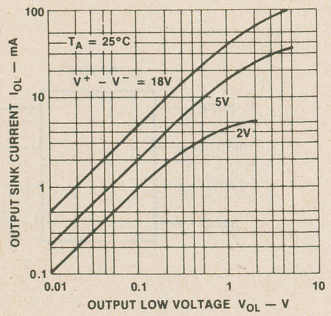
Note: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than $V^+ + 0.3V$ or less than $V^- - 0.3V$ may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the 7555 must be turned on first.

TRUTH TABLE

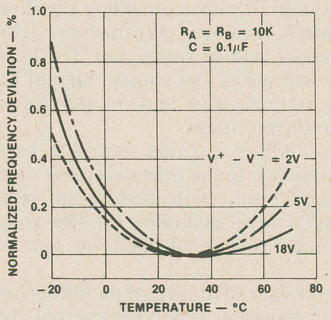
THRESHOLD VOLTAGE	TRIGGER VOLTAGE	RESET	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
$>2/3(V^+ - V^-)$	$>2/3(V^+ - V^-)$	HIGH	LOW	ON
$1/3<V_{TH}<2/3$	$1/3<V_{TH}<2/3$	HIGH	?	?
$<1/3(V^+ - V^-)$	$<1/3(V^+ - V^-)$	HIGH	HIGH	OFF

7555 276-1743

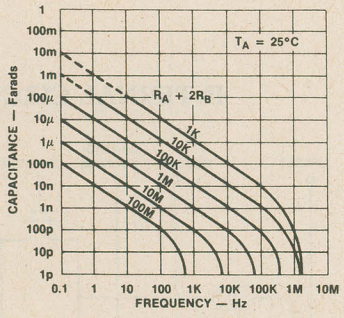
TYPICAL CHARACTERISTICS



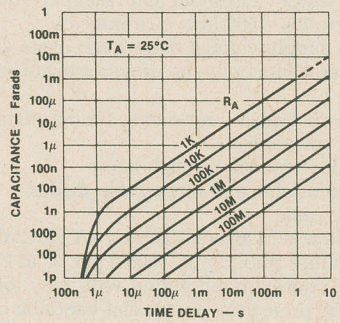
Output Sink Current vs Output Low Voltage



Normalized Frequency Deviation vs Temperature



Capacitance vs Free-Running Frequency



Capacitance vs Time Delay

TYPICAL APPLICATIONS

Astable Operation (Figure 1)

The circuit can be connected to trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 and 2/3 $(V^+ - V^-)$. As in the triggered mode, the charge and discharge times, and therefore the frequency, are essentially independent of the supply voltage.

The frequency of oscillation is given by: $$f = \frac{1}{t} = \frac{1.46}{(R_A + 2\,R_B)\,C}$$

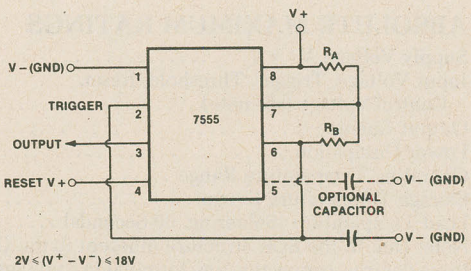


Figure 1—Astable Operation

Monstable Operation (Figure 2)

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative trigger pulse to pin 2, the flip flop is set which releases the short curcuit across the external capacitor and drives the output high. The voltage across the capacitor now increases exponentially with a time constant $\tau = R_A C$. When the voltage across the capacitor equals 2/3 $(V^+ - V^-)$, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the output to its low state.

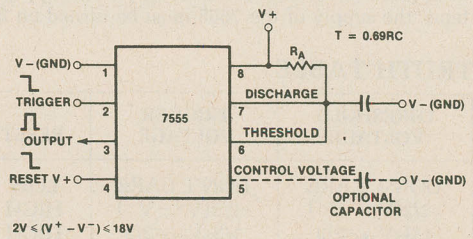
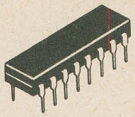


Figure 2—Monostable Operation



PROGRAMMABLE ANALOG COMPANDOR

NE572
276-1781

GENERAL DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

FEATURES

- Independent control of attack and recovery time.
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external Op Amp
- Wide dynamic range — greater than 110 dB
- Temperature compensated gain control
- Low distortion gain cell
- Low noise — 6μV typical
- Wide supply voltage range — 6 to 22 V
- System level adjustable with external components.

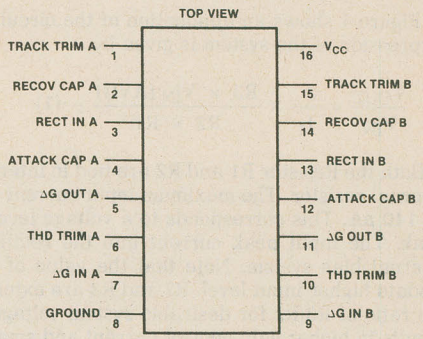
APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High level limiter
- Low level noise gate
- State variable filter

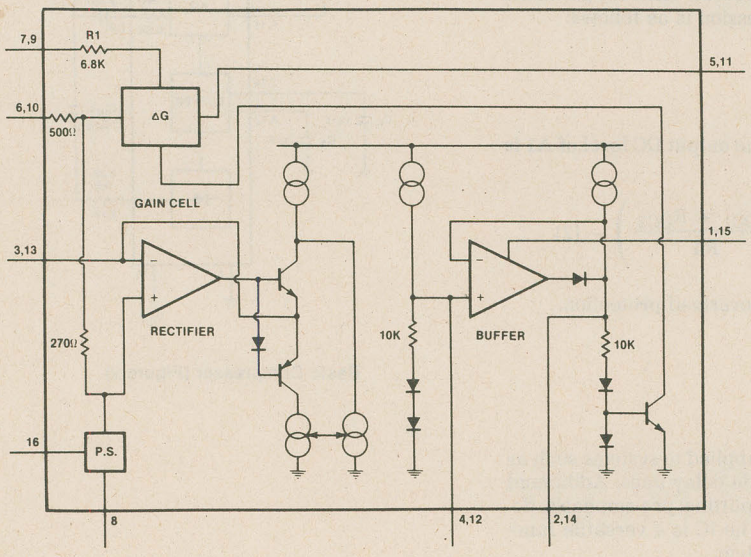
ABSOLUTE MAXIMUM RATINGS

Supply voltage . . . . . 22 V
Operating temperature range . . . . . 0 to 70°C
Power dissipation . . . . . 500 mW

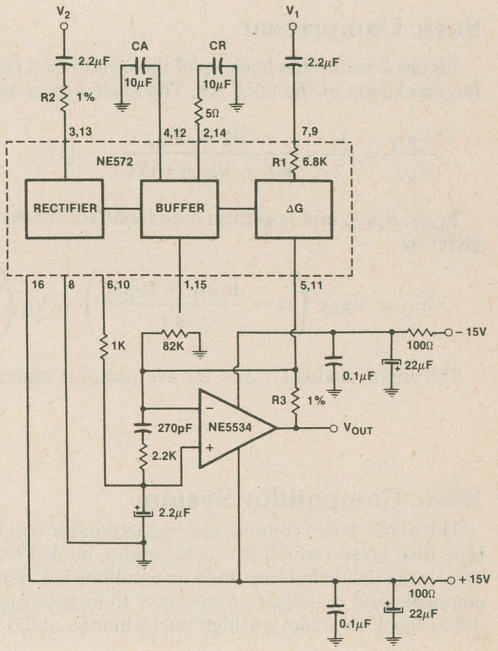
PIN CONNECTION



BLOCK DIAGRAM



TEST CIRCUIT



Test Circuit

NE572 276-1781

TYPICAL APPLICATIONS

Basic Expandor

Figure 1 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

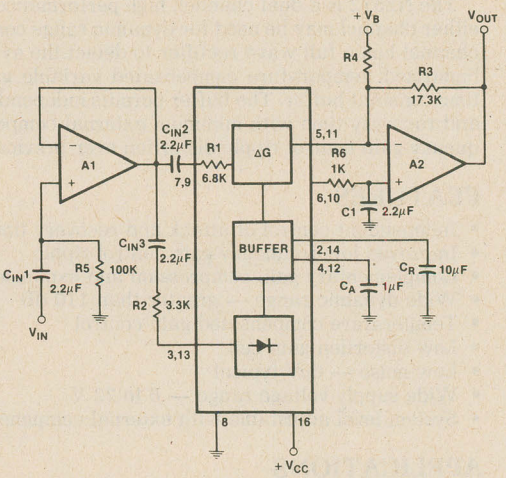
$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \times \frac{R3 \times V_{IN}(AVG)}{R2 \times R1} \quad - (1)$$

Both the Resistor R1 and R2 are tied to internal summing nodes. R1 is a 6.8 K internal resistor. The maximum input current into the gain cell can be as large as 140 μA. This corresponds to a voltage level of 140 μA $\times$ 6.8 K = 952 mV peak. The input peak current into the rectifier is limited to 300 μA by the internal bias system. Note that the value of R1 can be increased to accommodate higher input level. R2 and R3 are external resistors. It is easy to adjust the ratio of R3/R2 for desirable system voltage and current levels. A small R2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A2. R3 and A2 convert the gain cell output current to the output voltage. In high performance applications, A2 has to be low noise, high speed and wide band so that the high performance output of the gain cell will not be degraded. The non-inverting input of A2 can be biased at the low noise internal reference pin 6 or 10. Resistor R4 is used to biased up the output DC level of A2 for maximum swing. The output DC level of A2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R3}{R4}\right) - V_B\left(\frac{R3}{R4}\right) \quad - (2)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.



Basic Expandor (Figure 1)

Basic Compressor

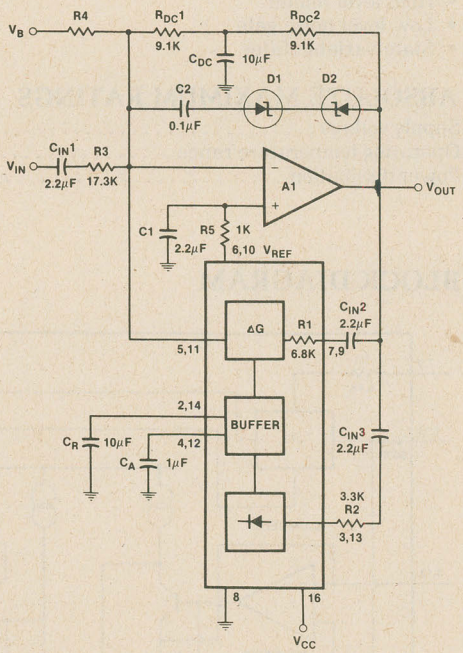
Figure 2 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{I_1}{2} \times \frac{R2 \times R1}{R3 \times V_{OUT}(AVG)} \quad - (1)$$

R_{DC1}, R_{DC2}, and C_{DC} form a dc feedback for A1. The output DC level of A1 is given by

$$C_{DC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R4}\right) - V_B\left(\frac{R_{DC1} + R_{DC2}}{R4}\right) \quad - (2)$$

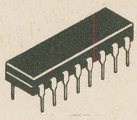
The zener diodes D1 and D2 are used for channel overload protection.



Basic Compressor (Figure 2)

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system.



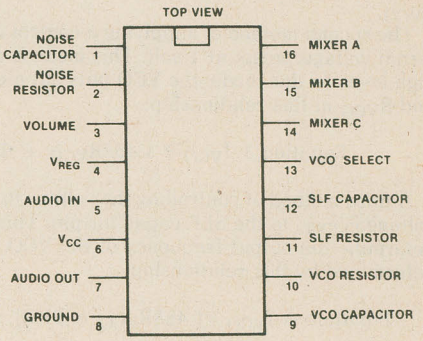
COMPLEX SOUND GENERATOR

SN94281
276-1767

GENERAL DESCRIPTION

The SN94281 complex sound generator is a monolithic chip combining both analog (bipolar) and digital (I2L) circuitry. It includes a noise generator, a voltage-controlled oscillator (VCO), and a super-low-frequency oscillator (SLF) together with a noise filter, mixer, audio amplifier, and control circuitry to provide noise, tone, or low-frequency sounds and any combinations of these. Programming is accomplished via control inputs and user-defined external components, which allows a wide variety of sound to be created and tailored for particular applications. This device may be used in a variety of applications requiring audio feedback to the operator including entertainment equipment such as arcade or home video games, pinball games, toys; consumer-oriented equipment such as timers, alarms, and controls.

PIN CONNECTION



FEATURES

- Generates noise, tone, or low frequency based sounds, or combinations of these
- Sounds are defined by user via external components
- Allows custom sounds to be created easily
- Low power requirements
- Allows multiple sound system
- Compatible with microprocessor systems
- On board 125 MW audio amplifier

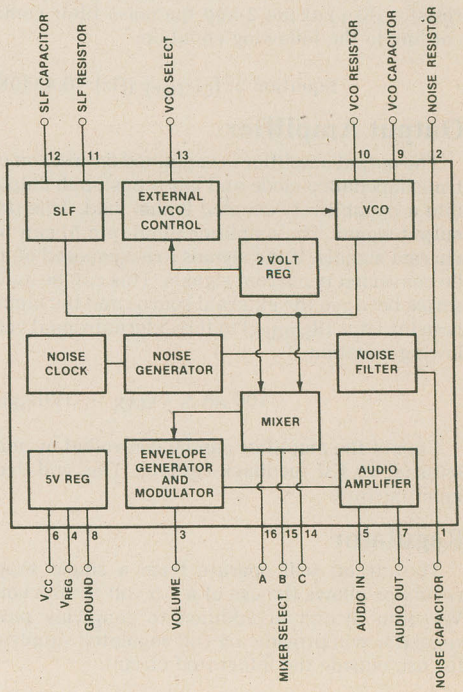
APPLICATIONS

- Home video games
- Pinball games
- Timers
- Alarms
- Toys

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... 12 V
Input Voltage: Logic Input ..... 12 V
Capacitor Input ..... 5 V
Resistor Input ..... 5 V
Operating Ambient Temperature Range ..... 0 to +70°C
Storage Temperature Range ..... −65 to +150°C

BLOCK DIAGRAM



OPERATION

Super Low Frequency Oscillator (SLF)

The SLF is normally operated in the range of 0.1 to 30 hertz, but will operate up to 20 kHz. The frequency is determined by two external components, the SLF control resistor (R_{SLF}) at pin 11 at ground and the SLF control capacitor (C_{SLF}) at pin 12 at ground according to the following equation:

Equation 1: SLF Frequency (Hz) $\cong 0.66/(9K\Omega + R_{SLF}) \times C_{SLF}$ at $V_{REG} = 5V$

The SLF supplies two signals to other parts of the device. It feeds a 50% duty cycle square wave to the mixer, and it feeds a triangular wave to the external VCO of SLF select logic, where, if VCO select (pin 13) is at a low logic level, it is fed through to the VCO to modulate the frequency of that oscillator.

Voltage Controlled Oscillator (VCO)

The VCO produces a tone output whose frequency is dependent upon the voltage at the input of the VCO. This controlling voltage may be either the SLF output described above, an internal voltage producing a constant tone, or externally by placing a voltage on the SLF capacitor pin. The higher the voltage applied to the VCO, the lower the frequency of the VCO output.

The first mode, VCO controlled by SLF, is selected by placing the VCO select pin low and supplying both the VCO capacitor (CVCO) at pin 9 at ground and the VCO resistor (R_{VCO}) at pin 10 at ground. Minimum frequency of the VCO is determined by the following equation:

Equation 2: Minimum VCO Frequency (Hz) $\cong 0.60/(9K\Omega + R_{VCO}) \times C_{VCO}$

The frequency range of the VCO is internally determined at an approximate ratio of 10:1, so that maximum frequency of the VCO will be approximately ten

SN94281 276-1767

OPERATION (Cont'd)

times the minimum frequency determined by the external components R_{VCO} and C_{VCO}.

The second method of supplying a control voltage for the VCO is to use an internal voltage preset at 1 volt. This mode is selected by taking VCO select to a high level. In this mode, the VCO puts out a constant tone determined by C_{VCO} and R_{VCO} in this relationship:

Equation 3: $f_{VCO} \cong 1.45/(R_{VCO} + 9K\Omega) \times C_{VCO} \times 0.9V$ Hz

A third method of controlling the voltage to the VCO is to apply the controlling voltage (V_{EXT}) to the SLF capacitor pin. This voltage level (0 to 2.30 volts) will determine the output frequency of the VCO. Output frequency in this mode is determined by this relationship:

Equation 4: $f_{VCO} \cong 1.45/(R_{VCO} + 9K\Omega) \times C_{VCO} \times (V_{EXT} - 0.1V)$ Hz

Mixer

To obtain two sounds occurring simultaneously (e.g., car engine and siren or steam engine and whistle), multiplexing is required. The multiplexing is accomplished by switching the mixer select lines at a sufficiently rapid rate that the two sounds seem to occur at the same time. The frequency of the multiplexing should be above the human hearing range. A multiplexing drive signal with a 50% duty cycle is required to provide equal amplitudes for both sound functions.

Volume

Output volume from the 94281 can be controlled by varying a voltage level on pin 3. This voltage level should range from 3.5 volts, for maximum volume, to 0.4 volts or below for no output. Under no circumstances should this pin be taken above 5 volts or below 0 volts. Voltages outside of this range could damage the unit.

Noise Generator/Filter

The noise generator produces psuedo-random white noise that passes through the noise filter before being applied to the mixer. The variable-bandwidth low-pass filter has its cutoff point defined by the noise filter control resistor (R_{NF}) at pin 2 and the noise filter control capacitor (C_{NF}) at pin 1 according to the following equation:

Equation 5: f_{CUTOFF} (Hz) $\cong 0.43/(9K\Omega + R_{NF}) \times C_{NF}$

Output Amplifier

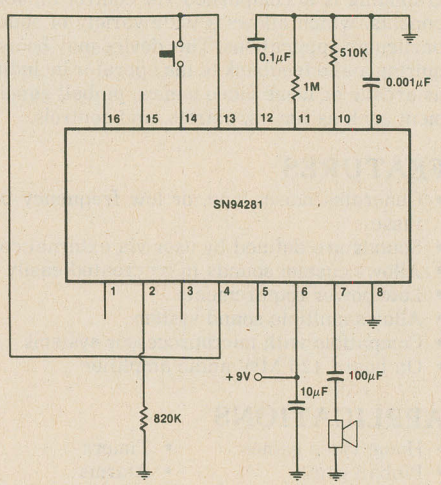
The output amplifier is contained entirely on chip. The amplifier operates in a transimpedance mode and has a push-pull output capable of delivering 125 mA into a capacitively coupled 8 ohm load. This produces a two volt peak-to-peak output signal. The amplifier input (pin 5) can be used to sum several external current signals. If the signals are composed of a varying voltage they must first be converted to current signals. This can be accomplished by using a resistor in series between the external source and the input (pin 5). The relationship of this resistor vaue (R_{SERIES}) to the external signal voltage (V_{MAX}) is given by the following equation:

$$-100\ \mu A < V_{MAX} - 3V/R_{SERIES} < 100\ \mu A$$

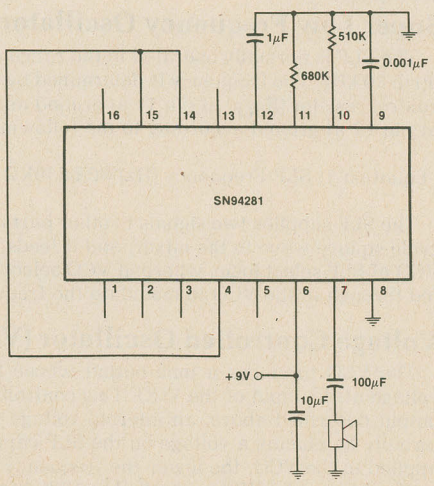
Gain of the amplifier can be controlled by adding a resistor in parallel to the internal 10 KΩ feedback resistor. This will decrease gain and allow a larger input current.

Regulator

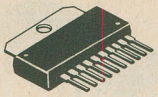
The circuit will operate from a single supply (pin 6). An internal 5 volt regulator allows the use of a 7.5 volt to 10.5 volt unregulated supply applied to V_{CC} (pin 6) and in addition to supplying power for the chip, the internal regulator will provide a 5 volt regulated supply of up to 5 mA from V_{REG} (pin 4) for use outside the integrated circuit.



Train with Whistle



Bird Sound



5.8W AUDIO POWER AMPLIFIER

TA7205AP
276-705

GENERAL DESCRIPTION

The TA7205AP is a monolithic audio power amplifier with a built in thermal shut-down circuit designed for car radio and stereo applications.

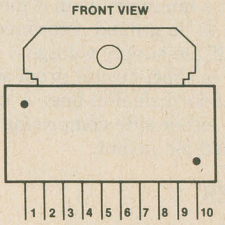
FEATURES

- Low distortion
  THD=0.15% (Typ.) (@P_{OUT}=1W, G_V=55dB)
  THD=0.07% (Typ.) (@P_{OUT}=1W, G_V=44dB)
- Operating supply voltage range: V_{CC}=9~18V
- 'PCT' process to insure low noise characteristic
- Current limiting for short-circuit protection
- Built in thermal shut-down circuit
- Built in surge voltage protection circuit

ABSOLUTE MAXIMUM RATINGS

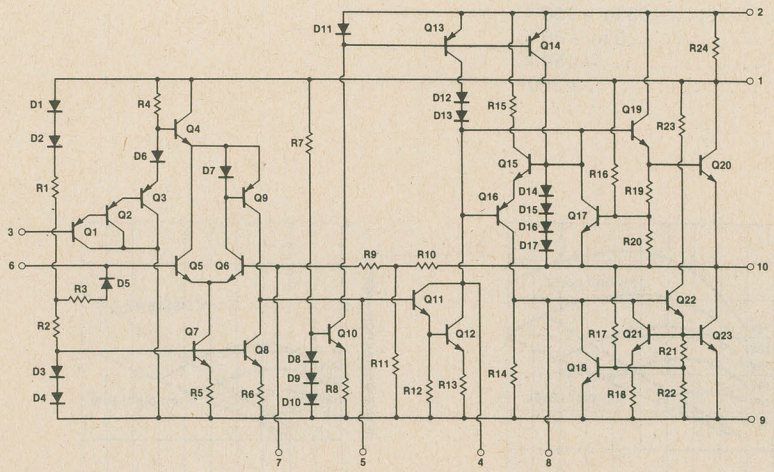
Operating Supply Voltage(V_{CC})	18V
Quiescent Supply Voltage (V_{CCQ})	25V
Output Peak Current (I_O)	4.5A
Quiescent Current (I_{CCQ})	80mA
Operating Temperature	−20 to +75°C
Storage Temperature	−55 to +150°C

PIN CONNECTION

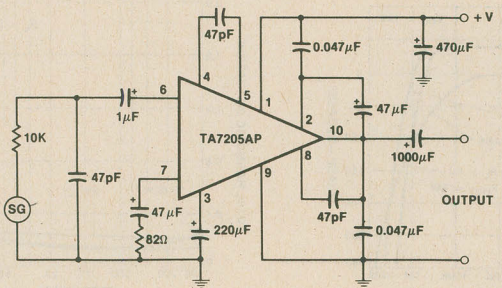


PIN	FUNCTION
1	V+
2	BOOTSTRAP
3	DECOUPLING
4	PHASE COMPENSATION
5	PHASE COMPENSATION
6	INPUT
7	NEGATIVE FEEDBACK
8	PHASE COMPENSATION
9	GROUND
10	OUTPUT

INTERNAL CIRCUIT

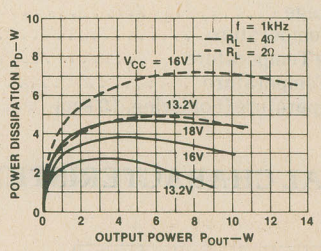


TYPICAL APPLICATION

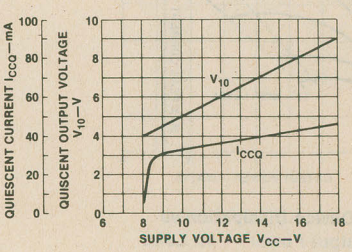


5 Watt Audio Amplifier

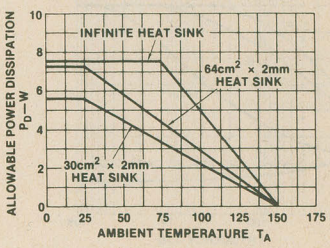
TYPICAL CHARACTERISTICS



Power Dissipation vs Output Power



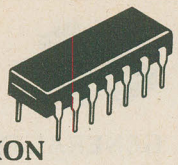
Quiescent Current and Output Voltage vs Supply Voltage



Allowable Power Dissipation vs Ambient Temperature

380
276-706

AUDIO POWER AMPLIFIER

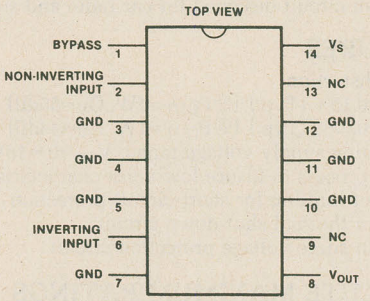


GENERAL DESCRIPTION

The 380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self centering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

PIN CONNECTION



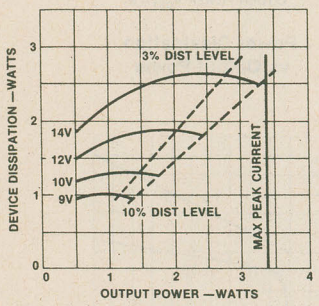
FEATURES

- Wide supply voltage range
- Low quiescent power drain
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage

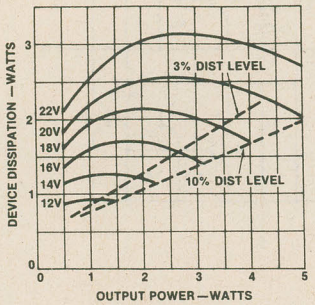
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	22 V
Peak Current	1.3 A
Package Dissipation 14-Pin DIP	10 W
Input Voltage	±0.5 V
Storage Temperature	−65 to +150°C
Operating Temperature	0 to +70°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec)	+300°

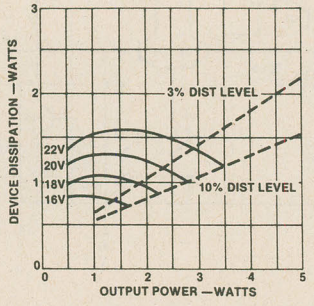
TYPICAL CHARACTERISTICS



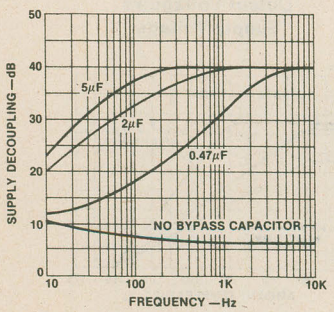
Device Dissipation vs Output Power — 4Ω Load



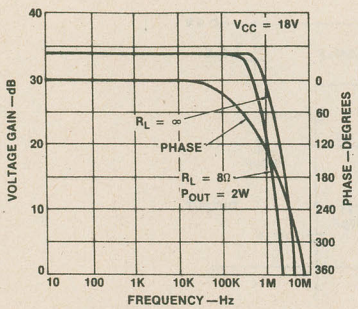
Device Dissipation vs Output Power — 8Ω Load



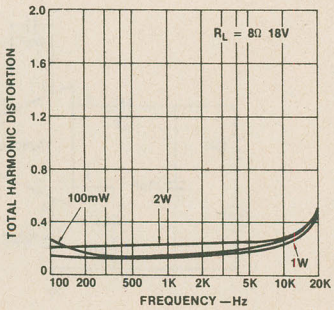
Device Dissipation vs Output Power — 16Ω Load



Supply Decoupling vs Frequency



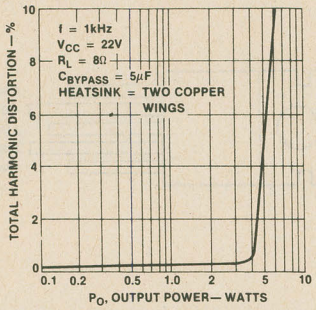
Output Voltage Gain and Phase vs Frequency



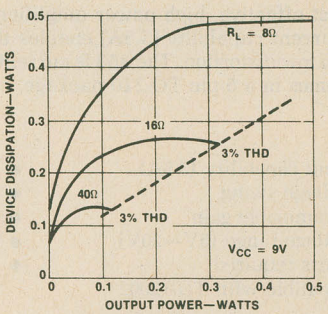
Total Harmonic Distortion vs Frequency

380 276-706

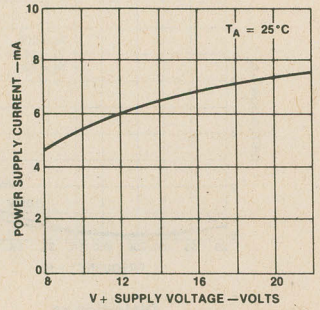
TYPICAL CHARACTERISTICS (Cont'd)



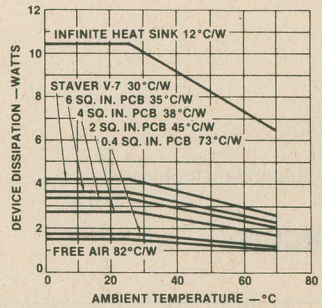
Total Harmonic Distortion vs Output Power



Device Dissipation vs Output Power

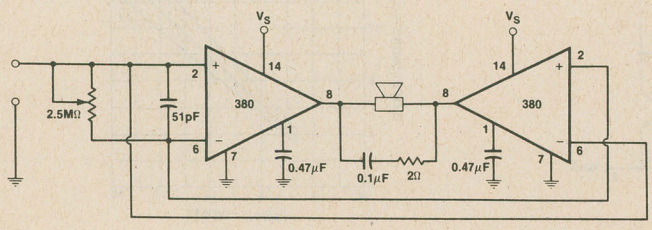


Power Supply Current vs Supply Voltage

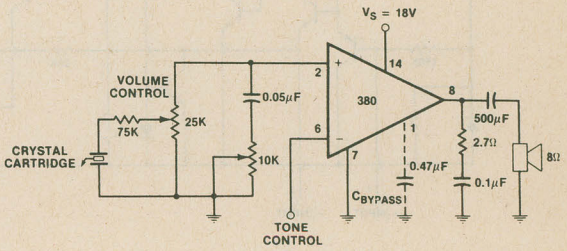


Device Dissipation vs Ambient Temperature

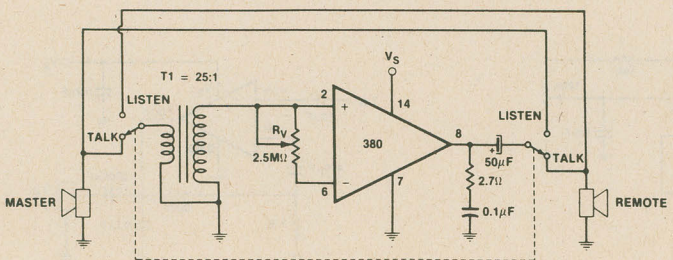
TYPICAL APPLICATIONS



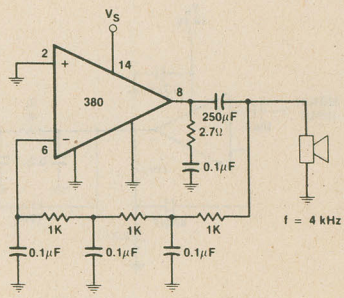
Bridge Amplifier



Phono Amplifier



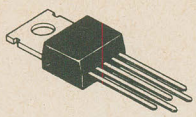
Intercom



Phase Shift Oscillator

383
276-703

8 WATT AUDIO POWER AMPLIFIER



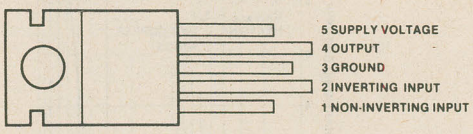
GENERAL DESCRIPTION

The 383 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The 383 is current limited and thermally protected. The 383 comes in a 5-pin TO-220 package.

FEATURES

- High peak current capability (3.5A)
- Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V—20V)
- Few external parts required
- Pin for pin compatible with TDA2002
- Low distortion
- High input impedance
- No turn-on transients
- Low noise
- Short circuit protected

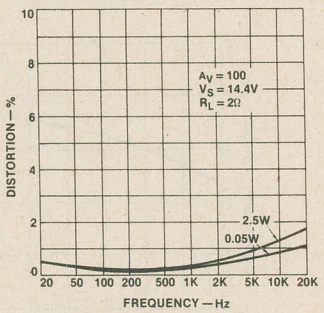
PIN CONNECTION



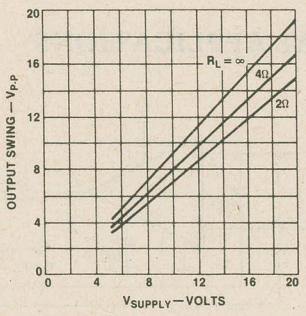
ABSOLUTE MAXIMUM RATINGS

Peak Supply Voltage (50 ms)	25V
Operating Supply Voltage	20V
Output Current	
Repetitive	3.5A
Non-repetitive	4.5A
Input Voltage	±0.5V
Power Dissipation	15W
Operating Temperature	0 to +70°C
Storage Temperature	−60 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

TYPICAL CHARACTERISTICS

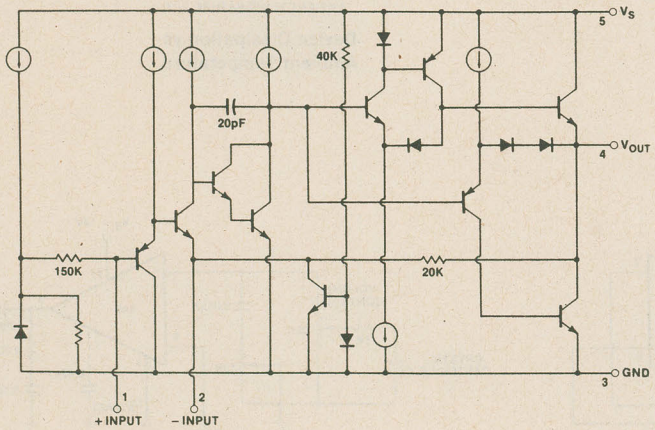


Distortion vs Frequency

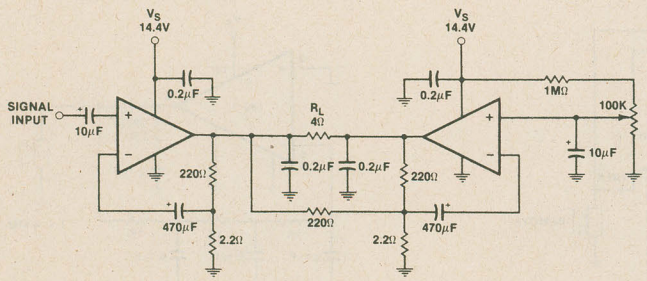


Output Swing vs Supply Voltage

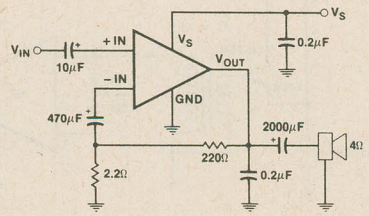
INTERNAL CIRCUIT



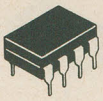
TYPICAL APPLICATIONS



16W Bridge Amplifier



Basic Audio Amp



LOW VOLTAGE AUDIO POWER AMPLIFIER

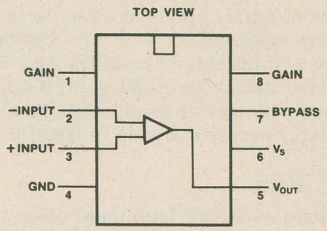
386
276-1731

GENERAL DESCRIPTION

The 386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 18 milli-watts when operating from a 6 volt supply, making the 386 ideal for battery operation.

PIN CONNECTION



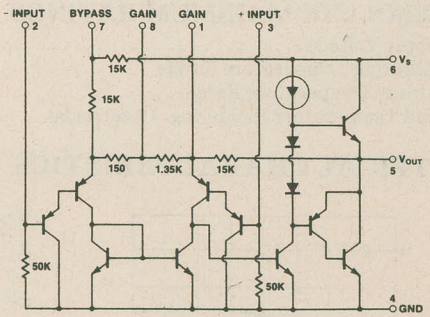
FEATURES

- Battery operation
- Minimum external parts
- Wide supply voltage range 4-12 volts
- Low quiescent current drain 3 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

APPLICATIONS

- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

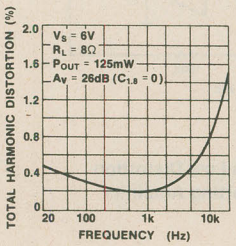
INTERNAL CIRCUIT



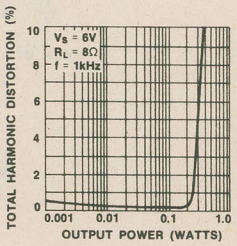
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15V
Package Dissipation 8 Pin DIP	660 mW
Input Voltage	±0.4V
Junction Temperature	+150°C
Operating Temperature	0 to +70°C
Storage Temperature	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

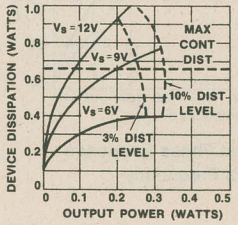
TYPICAL CHARACTERISTICS



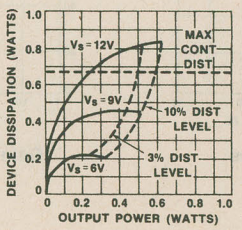
Distortion vs Frequency



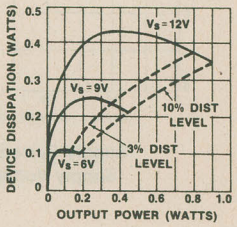
Distortion vs Output Power



Device Dissipation vs Output Power—4Ω Load

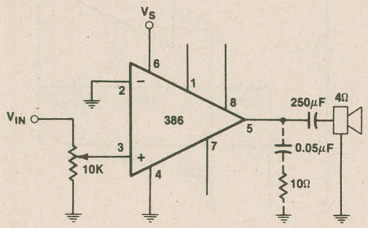


Device Dissipation vs Output Power—8Ω Load

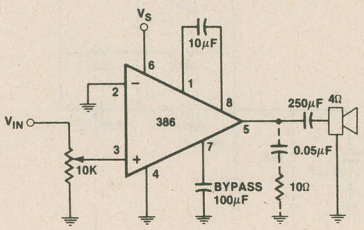


Device Dissipation vs Output Power—16Ω Load

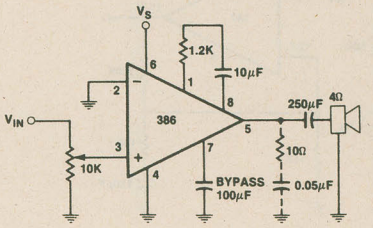
TYPICAL APPLICATIONS



Amplifier with Gain = 20 (Minimum Parts)



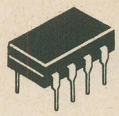
Amplifier with Gain = 50



Amplifier with Gain = 200

387
276-1737

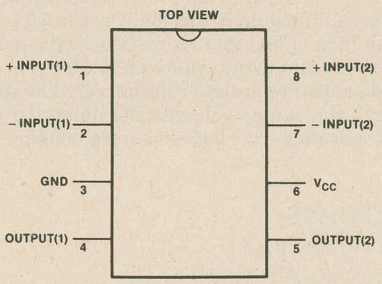
LOW NOISE DUAL PREAMPLIFIER



GENERAL DESCRIPTION

The 387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (104 dB), large output voltage swing (V_{CC} – 2 V) $_{P\text{-}P}$, and wide power band width (75 kHz, 20 $V_{P\text{-}P}$). The 387 operates from a single supply across the wide range of 9 to 30 V.

PIN CONNECTION



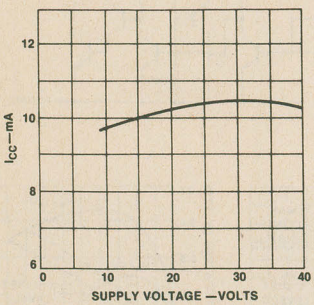
FEATURES

- Low noise — 0.8 μV total input noise
- High gain — 104 dB open loop
- Wide supply range — 9 to 30 V
- Power supply rejection — 110 dB
- Large output voltage swing (V_{CC} – 2 V) $_{P\text{-}P}$
- Wide band width 15 MHz unity gain
- Power band width 75 kHz, 20 $V_{P\text{-}P}$
- Internally compensated
- Short circuit protected

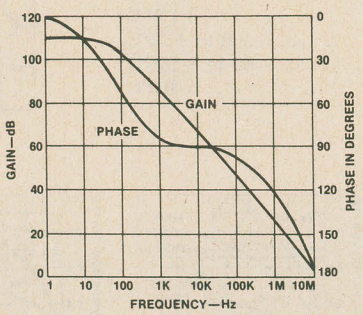
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... + 30 V
Operating Temperature Range ..... 0 to + 70°C
Storage Temperature Range ..... – 65 to + 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

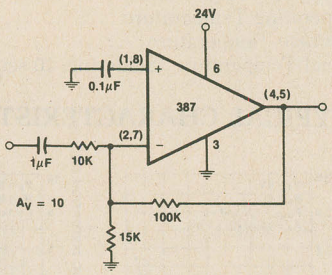
TYPICAL CHARACTERISTICS



Supply Current vs Supply Voltage

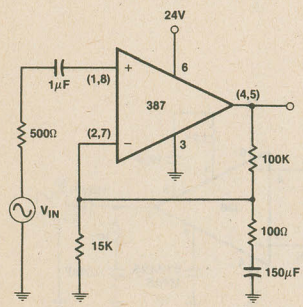


Gain and Phase Response vs Frequency

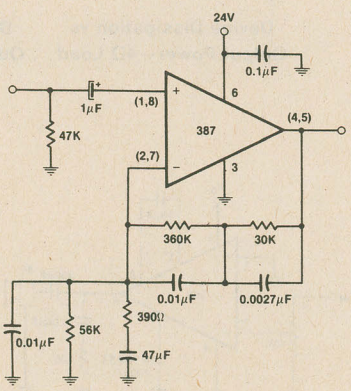


Ultra-Low Distortion Inverting Amplifier

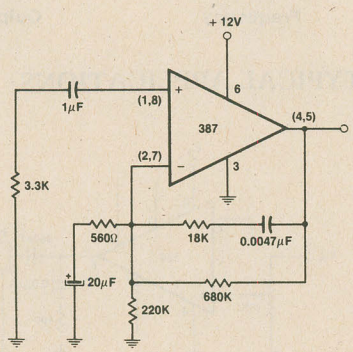
TYPICAL APPLICATIONS



Flat Gain Circuit (A_V = 1000)



Magnetic Phono Preamplifier



NAB Tape Circuit

LOW-LEVEL VIDEO DETECTOR

MC1330
276-1757

GENERAL DESCRIPTION

This is an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

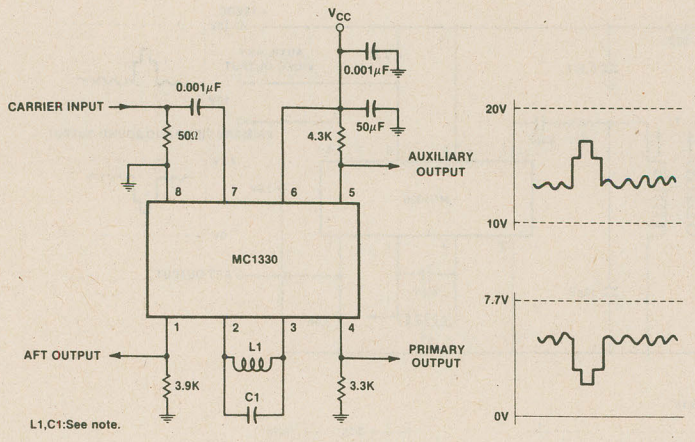
FEATURES

- Conversion gain—33 dB typical
- Excellent differential phase and gain
- High rejection of IF carrier feedthrough
- High video output—8.0 V p-p
- Fully balanced detector
- Output temperature compensated

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	24 Vdc
DC Video Output Current	5mAdc
DC AFT Output Current	2mAdc
Zero Signal dc Output Voltage (V_{cc}=+20 Vdc, Q=40, f_c=45.75 MHz)	
MC1330A1P	8.2 Vdc
MC1330A2P	9.0 Vdc
Supply Current	20mA
Maximum Signal dc Output Voltage (Pin 4)	0.5 Vdc
Conversion Gain for 1Vp-p Output (30% Modulation)	65mVrms
AFT Buffer Output at Carrier Frequency	650mVp-p
Junction Temperature	150°C
Operating Temperature Range (Ambient)	0 to +75°C
Storage Temperature Range	−65 to +150°C

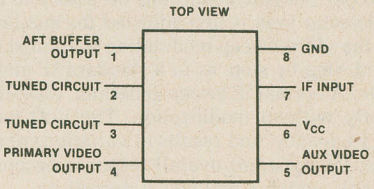
TYPICAL APPLICATIONS



NOTE: The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. See Figure 3. Values of Q from 20 to 50 recommended. (Note the internal resistance.)

Test Fixture Circuit

PIN CONNECTION



TYPICAL CHARACTERISTICS (V_{cc}=+20 Vdc)

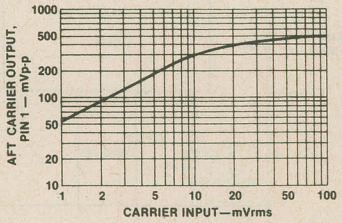


Figure 1

AFT Carrier Output vs Carrier Input

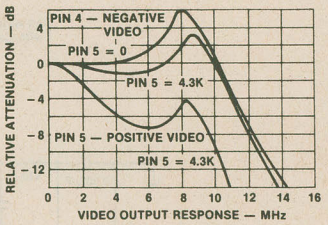
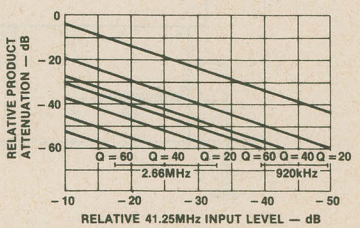


Figure 2

Relative Attenuation vs Video Output Response



REFERENCE = 3.58MHz OUTPUT
45.75MHz INPUT = 25mVrms
42.17MHz INPUT = 12.5mVrms
41.25MHz INPUT — RELATIVE TO 45.75 MHz INPUT = 4.5MHz

Figure 3

Relative Product Attenuation vs Relative 41.25 MHz Input Level

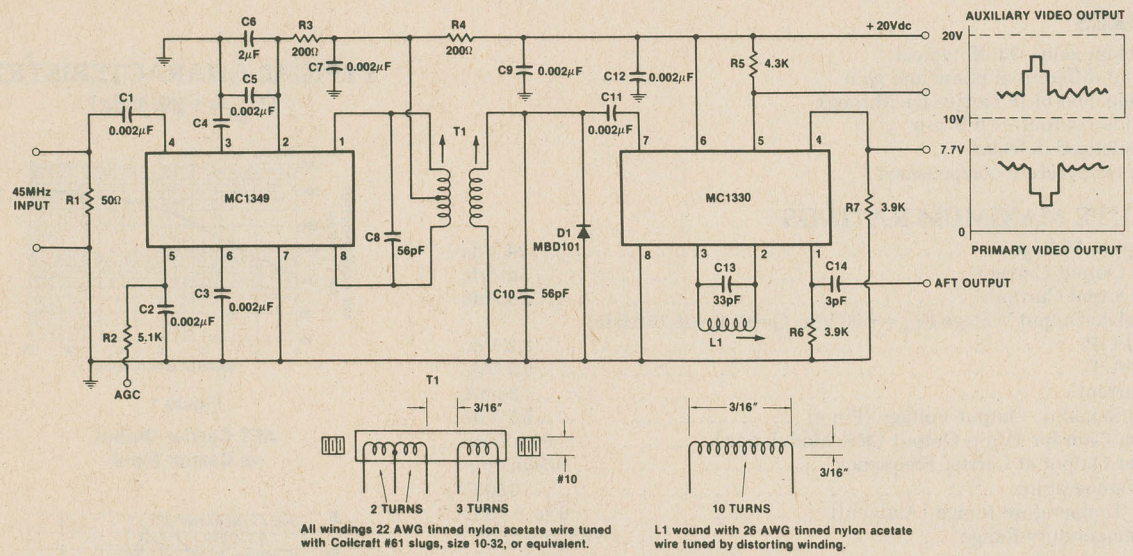
MC1330 276-1757

TYPICAL APPLICATIONS (Cont'd)

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

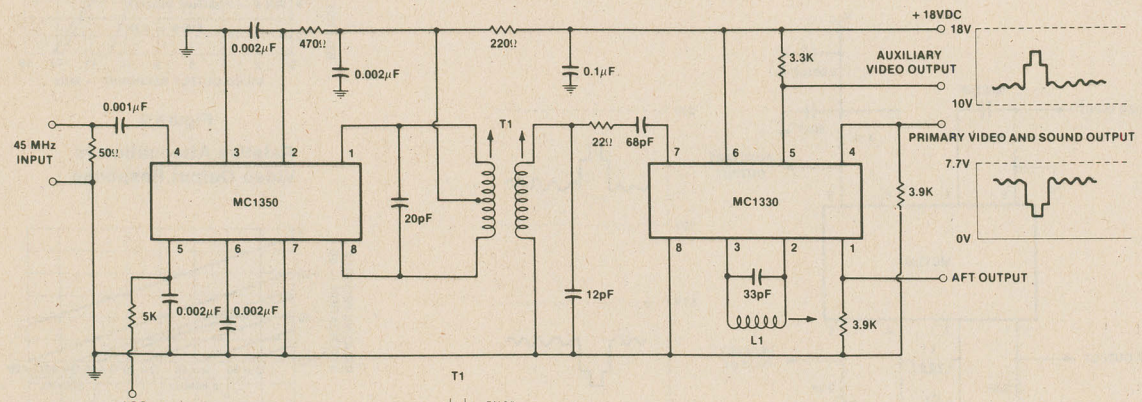
This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude.

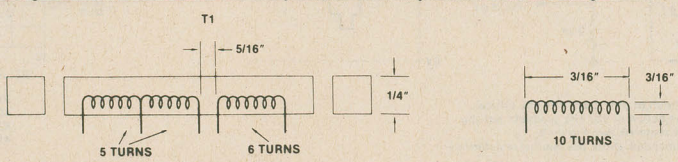


All windings 22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent.

L1 wound with 26 AWG tinned nylon acetate wire tuned by distorting winding.

Video IF Amplifier and Low-Level Detector





All windings #30 AWG tinned nylon acetate wire tuned with Arnold Type TH slugs.

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

Typical MC1350 Video IF Amplifier and MC1330 Low-Level Video Detector Circuit

IF AMPLIFIER

MC1350
276-1758

GENERAL DESCRIPTION

This monolithic IF amplifier is an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV.

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FEATURES

- Power gain — 50 dB typ at 45 MHz,
  — 48 dB typ at 58 MHz
- AGC range — 60 dB min. dc to 45 MHz
- Nearly constant input and output admittance over the entire AGC range
- y_{21} constant (−3.0 dB) to 90 MHz
- Low reverse transfer admittance — $\ll 1.0$ μmho typ
- 12-volt operation, single-polarity-power supply

ABSOLUTE MAXIMUM RATINGS

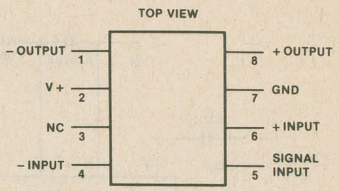
Power Supply Voltage	18Vdc
Power Dissipation	625mW
Operating Temperature Range	0 to +75°C

ELECTRICAL CHARACTERISTICS

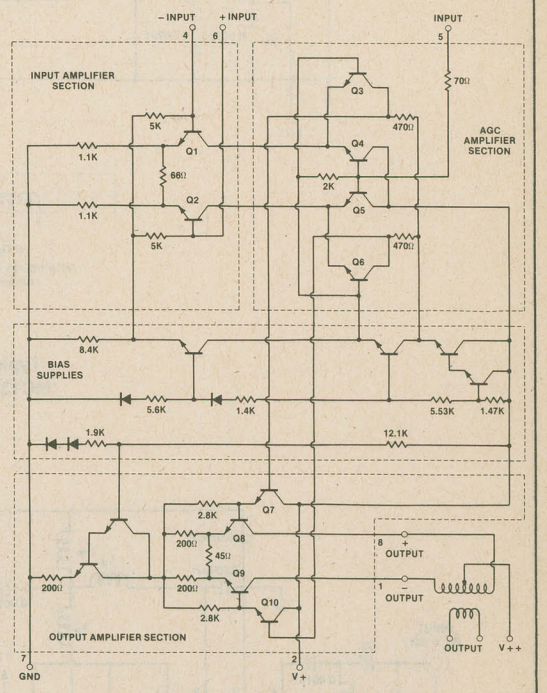
($V+ = +12$ Vdc; $T_A = +25°C$ unless otherwise noted)

Power Gain (Pin 5 grounded via a 5.1k resistor)	
f = 58 MHz, BW = 4.5 MHz	48dB
f = 45 MHz, BW = 4.5 MHz	50dB
f = 10.7 MHz, BW = 350 kHz	58dB
f = 455 kHz, BW = 20 kHz	62dB
Power Dissipation	204mW

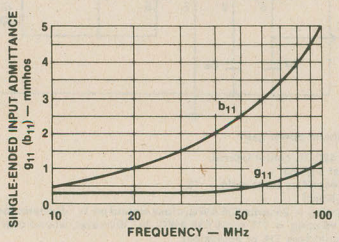
PIN CONNECTION



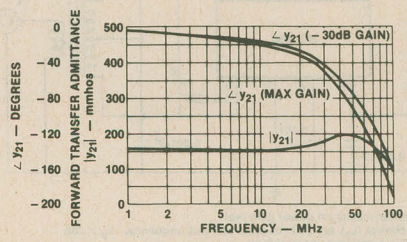
INTERNAL CIRCUIT



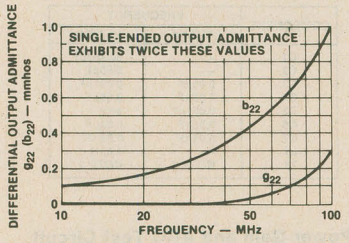
TYPICAL CHARACTERISTICS ($V+=12V$, $T_A=+25°C$)



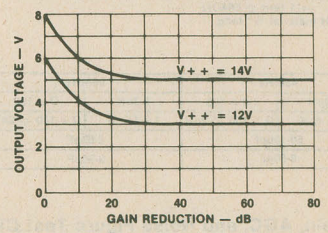
Input Admittance vs Frequency



Forward Transfer Admittance and Phase vs Frequency



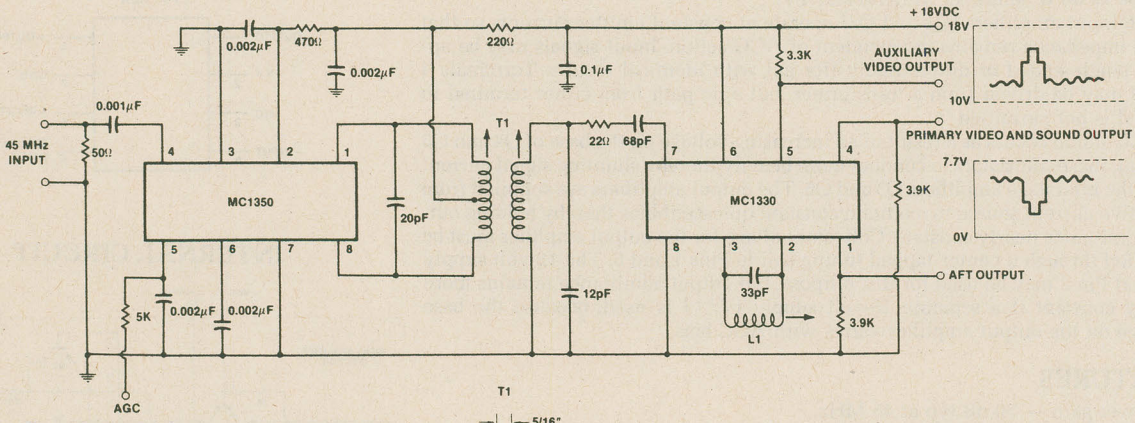
Differential Output Admittance vs Frequency

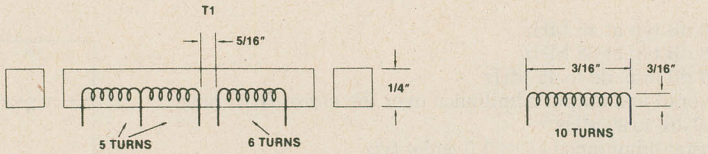


Differential Output Voltage vs Gain Reduction

MC1350 276-1758

TYPICAL APPLICATIONS

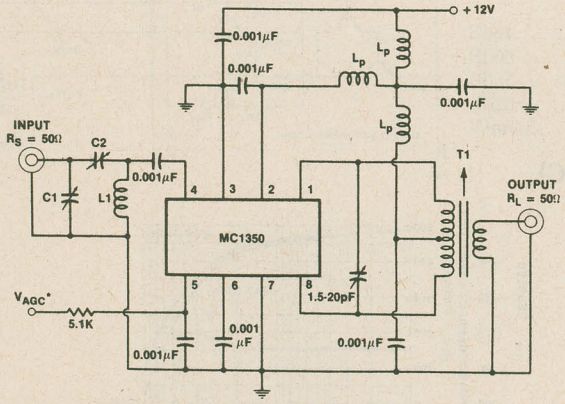




All windings #30 AWG tinned nylon acetate wire tuned with Arnold Type TH slugs.

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

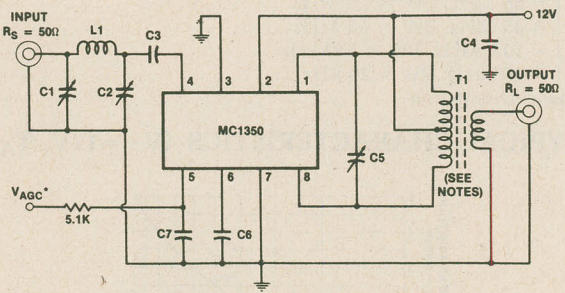
Typical MC1350 Video IF Amplifier and MC1330 Low-Level Video Detector Circuit



*Connect to ground for maximum power gain test.
All power-supply chokes (L_p), are self-resonate at input frequency. $L_p \geq 20K$
L1 @ 45 MHz = 7¼ turns on a ¼" coil form.
@ 58 MHz = 6 turns on a ¼" coil form.
T1 primary winding = 18 turns on a ¼" coil form, center-tapped.
secondary winding = 2 turns centered over primary winding @ 45MHz
= 1 turn @ 58MHz
Core = Arnold TH material ½" long.

	45MHz		58MHz	
L1	0.4μH	Q ≥ 100	0.3μH	Q ≥ 100
T1	1.3-3.4μH	Q ≥ 100 @ 2μH	1.2-3.8μH	Q ≥ 100 @ 2μH
C1	50-160pF		8-60pF	
C2	8-60pF		3-35pF	

Power Gain, AGC, and Noise Figure Test Circuit (45 MHz and 58 MHz)

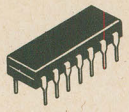


*Grounded for maximum power gain.

Note 1. Primary = 120μH, center-tapped.
Q_u = 140 at 455kHz.
Primary : Secondary turns ratio ≈ 13
2. Primary = 6.0μH
Primary winding = 24 turns #36 AWG, close wound on ¼" diameter form.
Secondary winding = 1½ turns #36 AWG, ¼" diameter, wound over center-tap.
Core = Arnold type TH, or equivalent.

COMPONENT	FREQUENCY	
	455kHz	10.7MHz
C1	—	80-450pF
C2	—	5-80pF
C3	0.05μF	0.001μF
C4	0.05μF	0.05μF
C5	0.001μF	36pF
C6	0.05μF	0.05μF
C7	0.05μF	0.05μF
L1	—	4.6μH
T1	NOTE 1	NOTE 2

Power Gain and AGC Test Circuit (455 kHz and 10.7 MHz)



IF AMPLIFIER, LIMITER, FM DETECTOR AUDIO DRIVER, ELECTRONIC ATTENUATOR

MC1358
276-1759

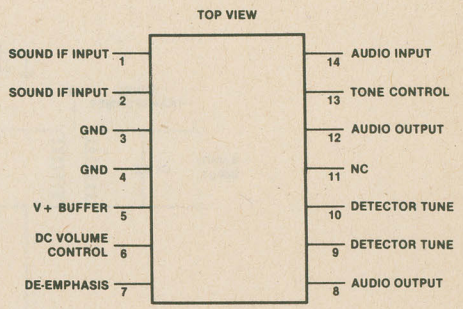
GENERAL DESCRIPTION

This TV sound IF amplifier is a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

FEATURES

- Differential peak detector requiring a single tuned circuit
- Electronic attenuator replaces conventional ac volume control — Range > 60 dB
- Excellent AM rejection at 4.5 and 5.5 MHz
- High stability
- Low harmonic distortion
- Audio drive capability — 6.0 mAp-p
- Minimum undesirable output signal @ maximum attenuation

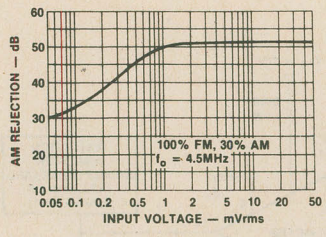
PIN CONNECTION



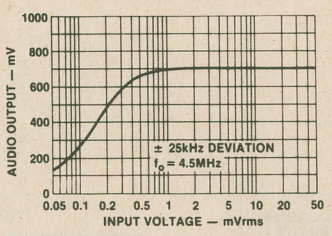
ABSOLUTE MAXIMUM RATINGS

Input Signal Voltage (Pins 1 and 2)	±3.0Vdc
Power Supply Current	50mA
Power Dissipation	625mW
Operating Temperature Range (Ambient)	−20 to +75°C
Storage Temperature Range	−65 to +150°C

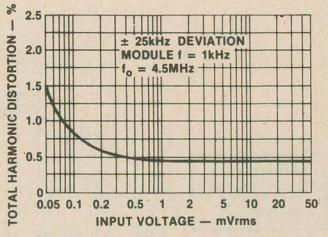
TYPICAL CHARACTERISTICS



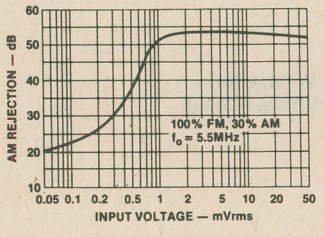
AM Rejection vs Input Voltage



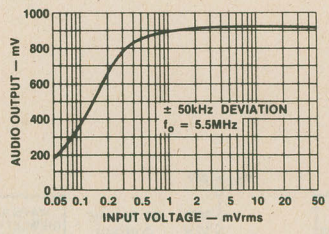
Audio Output vs Input Voltage



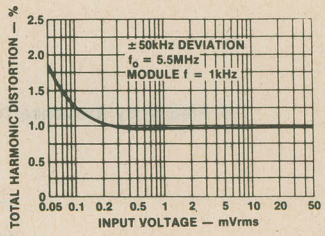
Total Harmonic Distortion vs Input Voltage



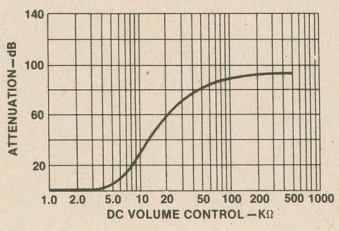
AM Rejection vs Input Voltage



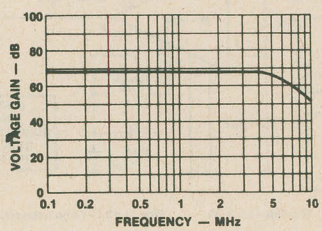
Audio Output vs Input Voltage



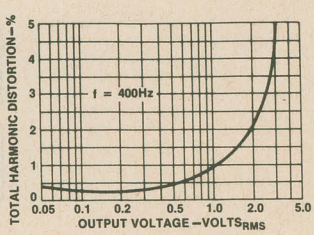
Total Harmonic Distortion vs Input Voltage



Attenuation vs DC Volume Control



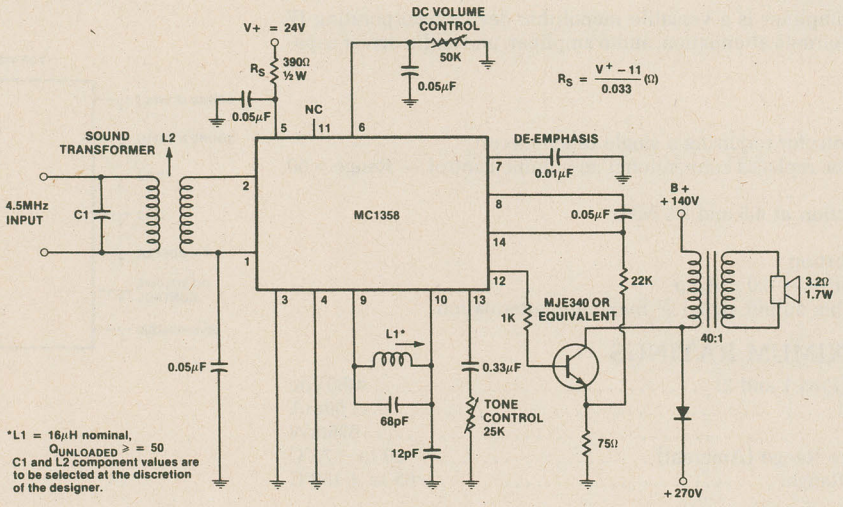
Voltage Gain vs IF Frequency



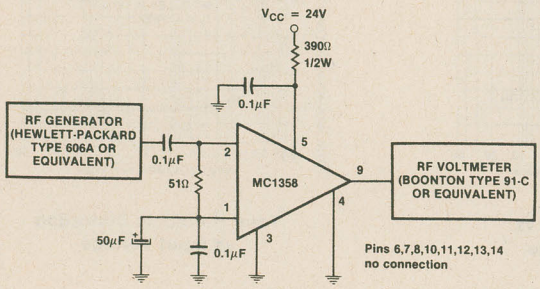
Total Harmonic Distortion vs Output Voltage

MC1358 276-1759

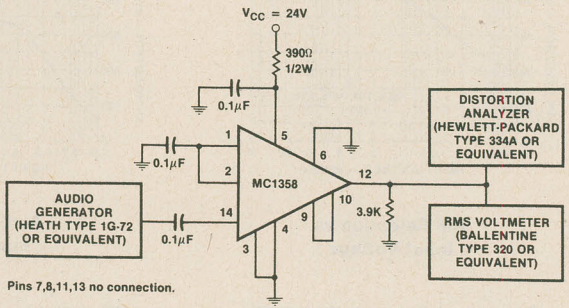
TYPICAL APPLICATIONS



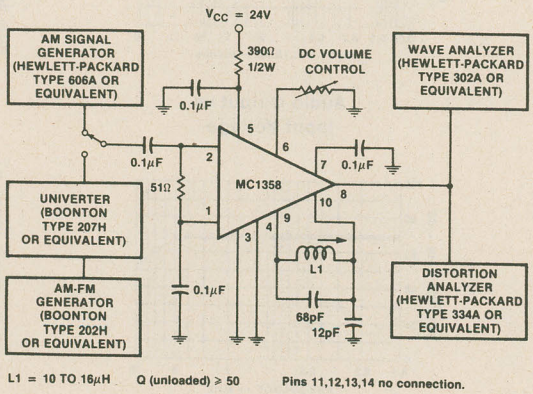
TV Application



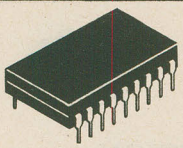
IF Frequency Response Test Circuit



Audio Voltage Gain, Audio THD Test Circuit



AM Rejection, Detected Audio, THD, Attenuation Test Circuit



DOT/BAR DISPLAY DRIVER

3916
276-1709

GENERAL DESCRIPTION

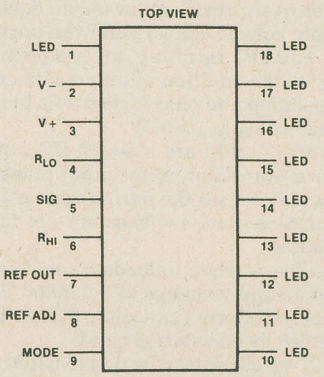
The 3916 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing an electronic version of the popular VU meter. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 0.2 dB.

Audio applications include average or peak level indicators, and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The 3916 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

PIN CONNECTION

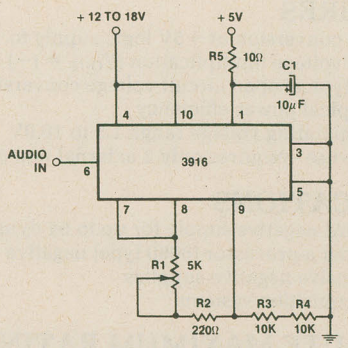


FEATURES

- Fast responding electronic VU meter
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 70 dB
- Internal voltage reference from 1.2V to 12V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

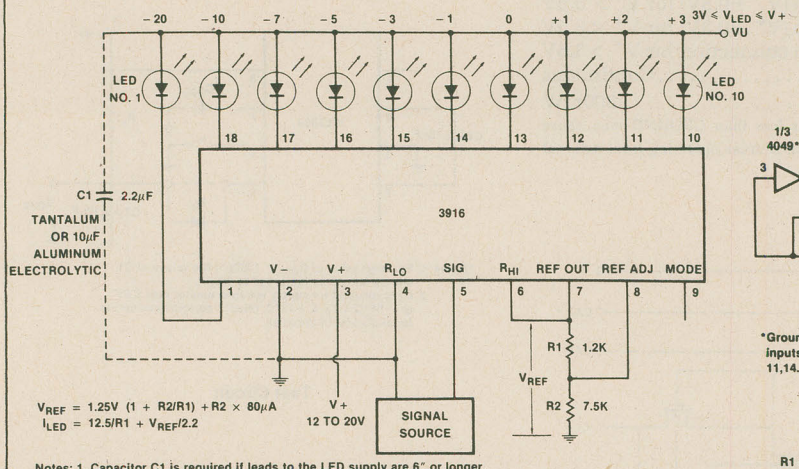
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 3 to 25 V
Input Signal Over Voltage ..... ± 35 V
Storage Temperature ..... 0 to 70°C



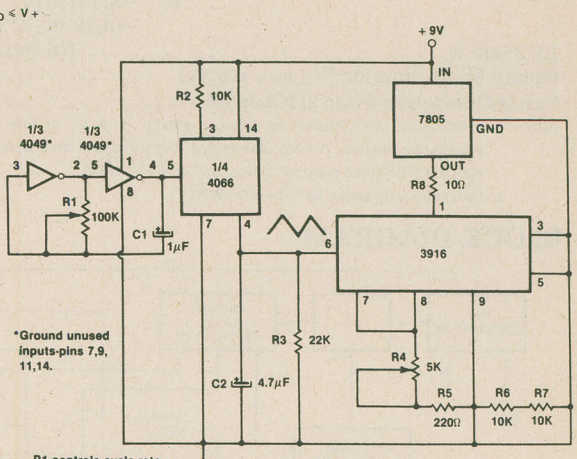
VU Bar Graph Display

TYPICAL APPLICATIONS



Notes: 1. Capacitor C1 is required if leads to the LED supply are 6" or longer.
2. Circuit as shown is wired for dot anode. For bar mode, connect pin 9 to pin 3.
I_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

0V to 10V VU Meter



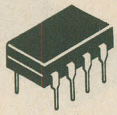
*Ground unused inputs-pins 7,9, 11,14.

R1 controls cycle rate.
R4 controls range.
Two gate oscillator switches 4066 on and off.
C2 is charged via R2 and discharged by R3 to give voltage ramp.

Back and Forth Flasher

ICL7660
276-2335

VOLTAGE CONVERTER



GENERAL DESCRIPTION

The ICL7660 is a power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5 to +10.0V, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only 2 non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for $V_{SUPPLY} > 6.5V$.

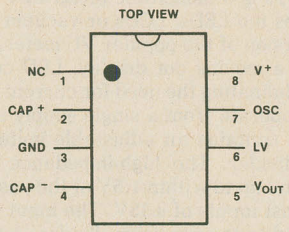
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Typical applications for the ICL7660 will be data acquisition and microprocessor based systems where there is a +5 volt supply available for the digital functions and an additional −5 volt supply is required for the analog functions. The ICL7660 is also ideally suited for providing low current, −5V body bias supply for dynamic RAMs.

PIN CONNECTION



FEATURES

- Simple conversion of +5V logic supply to ±5V supplies
- Simple voltage multiplication ($V_{OUT} = (-) nV_{IN}$)
- 99.9% typical open circuit voltage conversion efficiency
- 98% typical power efficiency
- Wide operating voltage range 1.5 to 10.0V
- Easy to use - requires only 2 external non-critical passive components

APPLICATIONS

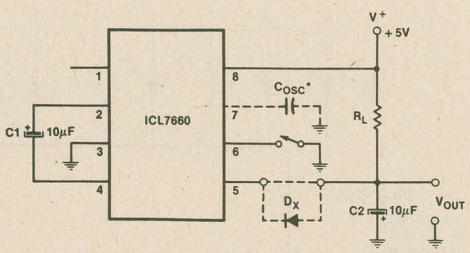
- On board negative supply for up to 64 dynamic RAMs.
- Localized μ-processor (8080 type) negative supplies
- Inexpensive negative supplies
- Data acquisition systems

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.5V
Oscillator Input Voltage (Note 1) .....−0.3V to (V^++0.3V) for $V^+ < 5.5V$
(V^+ −5.5V) to (V^+ +0.3V) for $V^+ > 5.5V$
−0.3V to (V^+ +0.3V) for $V^+ < 3.5V$
LV (Note 1)..... No connection for $V^+ > 3.5V$
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous
Power Dissipation (Note 2) ICL7660CPA 300mW

Notes: 1. Connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.
2. Derate linearly above 50°C by 5.5mW/°C.

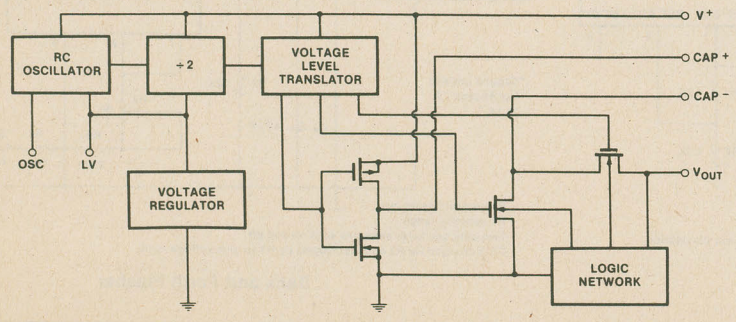
TEST CIRCUIT



*Notes: 1. For large value of C_{OSC} (> 1000pF) the values of C1 and C2 should be increased to 100μF.
2. D_X is required for supply voltages greater than 6.5V @ −55°C ≤ T_A ≤ +70°C; refer to performance curves for additional information.

Test Circuit

BLOCK DIAGRAM



ICL7660 276-2335

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A. The drive circuitry consumes minimal power
B. The output switches have extremely low ON resistance and virtually no offset.
C. The impedances of the pump and reservoir capacitors must be negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage multiplication if large values of C1 and C2 are used. ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS. The energy lost is defined by:

$$E = 1/2\ C1\ (V_1^2 - V_2^2)$$

Where V_1 and V_2 are the voltages on C1 during the pump and transfer cycles. If the impedances of C1 and C2 are relatively high at the pump frequency (refer to Fig. 1) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4. When using polarized capacitors, the + terminal of C1 must be connected to pin 2 of the ICL7660 and the + terminal of C2 must be connected to GROUND.
5. Add diode D_X as shown in the test circuit for hi-voltage, elevated temperature applications.

CONSIDERATIONS FOR HI VOLTAGE & ELEVATED TEMPERATURE

The ICL7660 will operate efficiently over its specified temperature range with only 2 external passive components (charge & pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70°C and 5.0 volts at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latch-up of the ICL7660. (Ref: Graph "Operating Voltage vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latch-up can be achieved by adding a general purpose diode in series with the ICL7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

TYPICAL APPLICATIONS

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 2 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of + 1.5V to + 10.0 volts, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltages and/or elevated temperatures.

The output characteristics of the circuit in Figure 2 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of −10mA and a supply voltage of +5 volts, the output voltage will be −4.3 volts. The dynamic output impedance due to the capacitor impedances is $1/\omega C$ where:

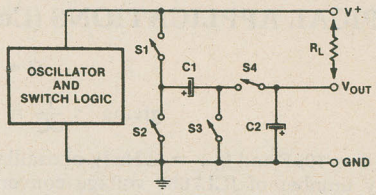
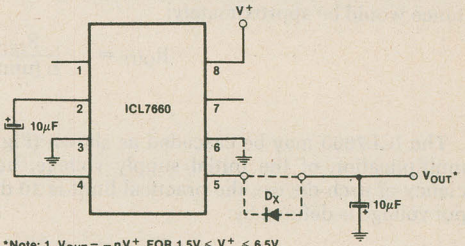


Figure 1—Idealized Voltage Doubler



*Note: 1. $V_{OUT} = -nV^+$ FOR $1.5V \leq V^+ \leq 6.5V$
2. $V_{OUT} = -n(V^+ - V_{FDX})$ FOR $6.5V \leq V^+ \leq 10V$

Figure 2—Simple Negative Converter

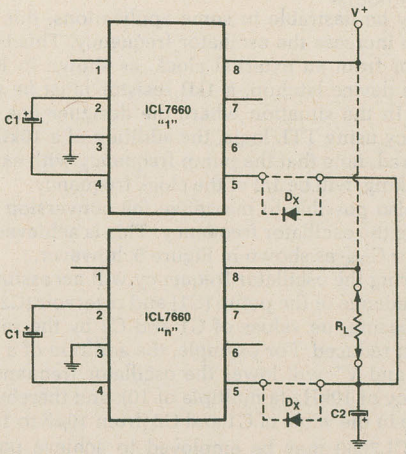
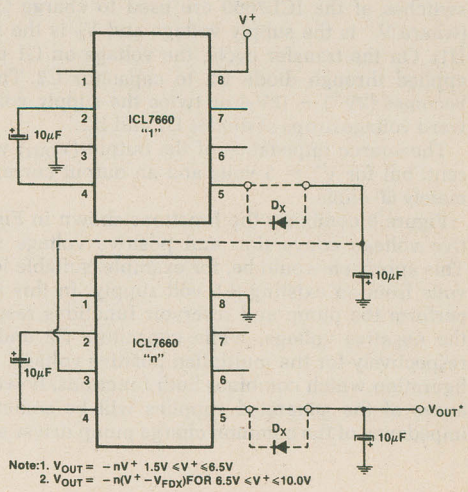


Figure 3—Paralleling Devices



Note:1. $V_{OUT} = -nV^+$ $1.5V \leq V^+ \leq 6.5V$
2. $V_{OUT} = -n(V^+ - V_{FDX})$ FOR $6.5V \leq V^+ \leq 10.0V$

Figure 4—Cascading Devices for Increased Output Voltage

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TYPICAL APPLICATIONS (Cont'd)

$$C = C1 = C2$$

$$\text{giving} \quad \frac{1}{\omega C} = \frac{1}{2\pi f_{OSC} \times 10^{-5}} = 3\ \Omega$$

for C = 10μF and f_{OSC} = 5kHz (½ of oscillator frequency)

Any number of ICL7660 voltage convertors may be paralleled (Fig. 3) to reduce output resistance. The reservoir capacitor, C2, serves all devices while each device requires its own pump capacitor, C1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7660})}{n\ (\text{number of devices})}$$

The ICL7660 may be cascaded as shown (Fig. 4) to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the sum of the individual ICL7660 R_{OUT}s.

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 5. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency.

It is also possible to maximize the conversion efficiency of the ICL7660 by lowering the oscillator frequency. This is achieved by connecting an additional capacitor C_{OSC} as shown in Figure 6, however.

Lowering the oscillator frequency will necessitate an undesirable increase in the impedance of the pump (C1) and reservoir (C2) capacitors; this is overcome by increasing the values of C1 and C2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C1 and C2 (from 10μF to 100μF).

The ICL7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 7. In this application, the pump inverter switches of the ICL7660 are used to charge C1 to a voltage level of V^+-V_F (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D1). On the transfer cycle, the voltage on C1 plus the supply voltage (V^+) is applied through diode D2 to capacitor C2. The voltage thus created on C2 becomes ($2V^+$) − ($2V_F$) or twice the supply voltage minus the combined forward voltage drops of diodes D1 and D2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V^+ = 5 volts and an output current of 10mA it will be approximately 60 ohms.

Figure 8 combines the functions shown in Figures 2 and 7 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C1 and C3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C2 and C4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

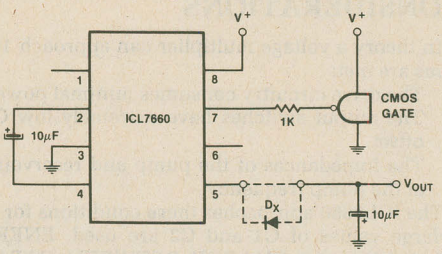


Figure 5—External Clocking

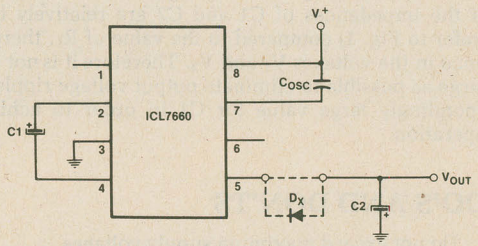
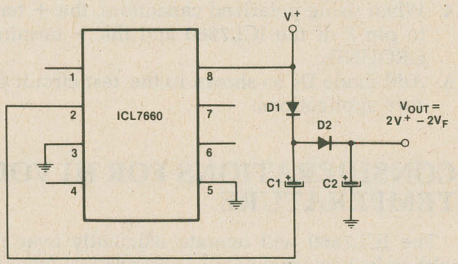


Figure 6—Lowering Oscillator Frequency



Note: D1 & D2 can be any suitable diode.

Figure 7—Positive Voltage Multiplier

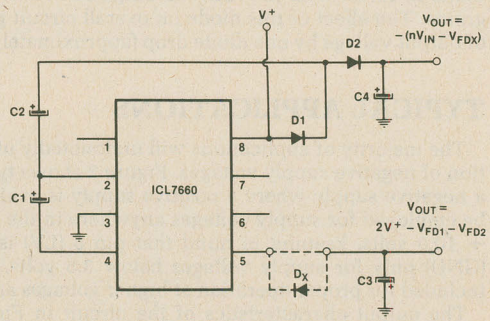


Figure 8—Combining Negative Converter and Positive Multiplier

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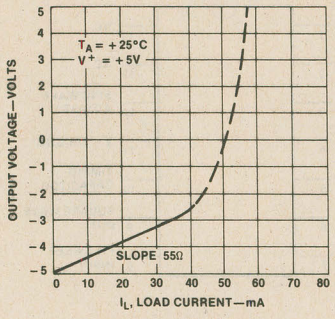
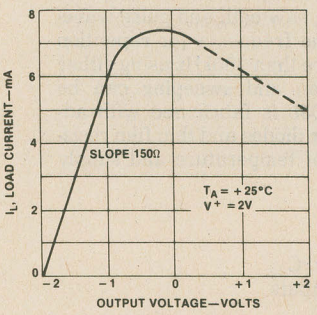
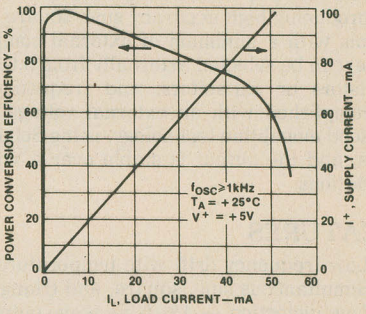
TYPICAL CHARACTERISTICS



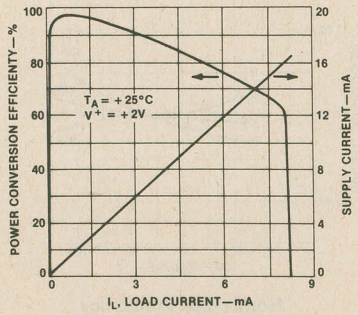
Output Voltage vs Load Current



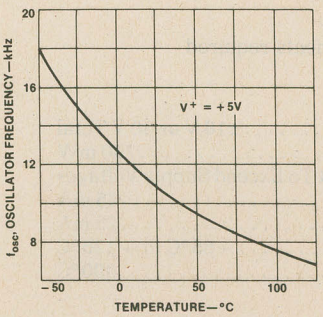
Output Voltage vs Load Current



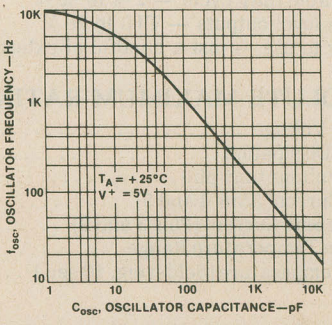
Power Conversion Efficiency vs Load Current



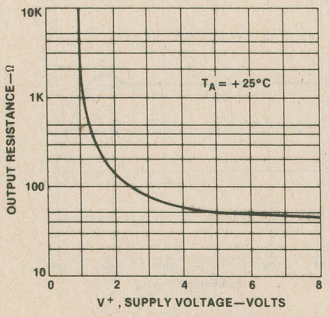
Power Conversion Efficiency vs Load Current



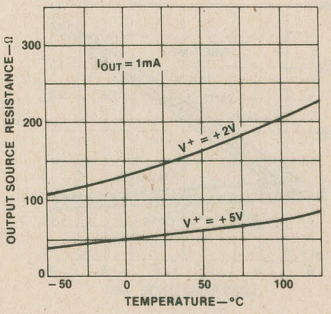
Oscillation Frequency vs Temperature



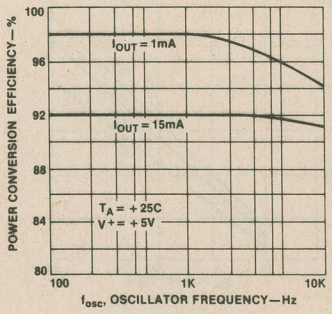
Oscillation Frequency vs External Oscillation Capacitance



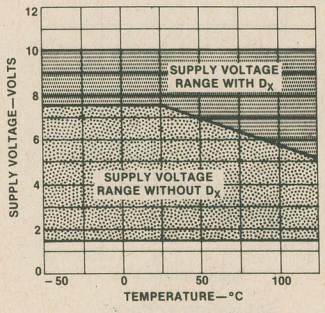
Output Source Resistance vs Supply Voltage



Output Source Resistance vs Temperature



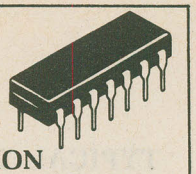
Power Conversion Efficiency vs Oscillation Frequency



Supply Voltage vs Temperature

ICL8038
276-2334

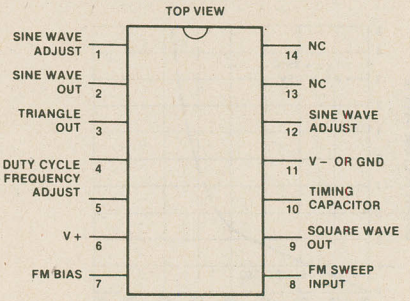
PRECISION WAVEFORM GENERATOR/ VOLTAGE CONTROLLED OSCILLATOR



GENERAL DESCRIPTION

The ICL8038 waveform generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from 0.001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations.

PIN CONNECTION

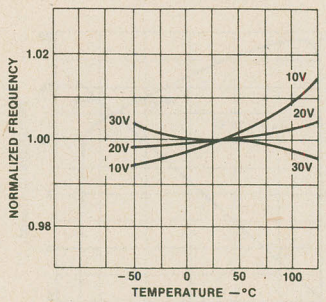


FEATURES

- Low frequency drift with temperature — 50ppm/°C
- Simultaneous sine, square, and triangle wave outputs
- Low distortion — 1% (sine wave output)
- High linearity — 0.1% (triangle wave output)
- Wide operating frequency range — 0.001Hz to 0.3MHz
- Variable duty cycle — 2% to 98%
- High level outputs — TTL to 28 V
- Easy to use — just a handful of external components required

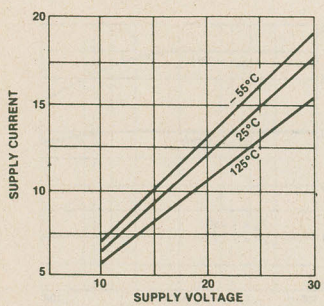
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V or 36 V Total
Power Dissipation	750 mW
Input Voltage (any pin)	Not To Exceed Supply Voltages
Input Current (Pins 4 and 5)	25 mA
Output Sink Current (Pins 3 and 9)	25 mA
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec.)	300°C

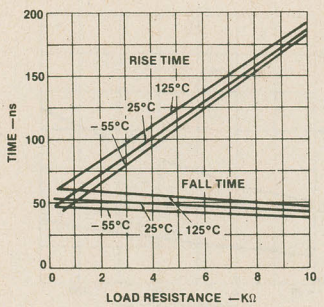


Normalized Frequency vs Temperature

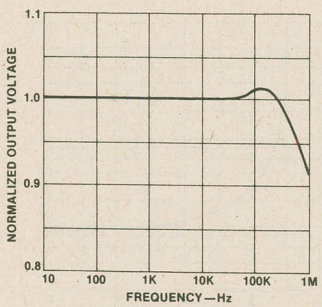
TYPICAL CHARACTERISTICS



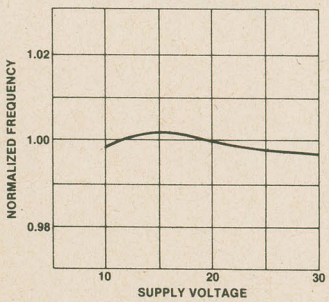
Supply Current vs Supply Voltage



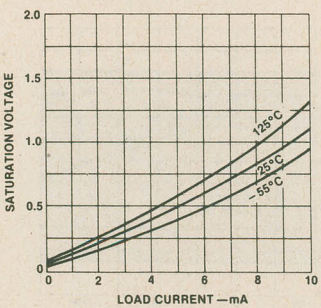
Time vs Load Resistance



Normalized Output Voltage vs Frequency

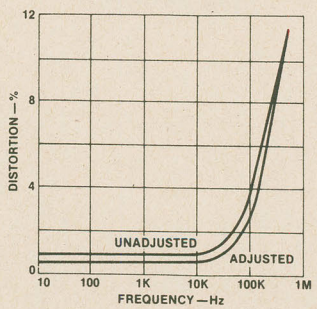


Normalized Frequency vs Supply Voltage



Saturation Voltage vs Load Current

Performance of the Square-Wave Output



Distortion vs Frequency

Performance of the Sine-Wave Output

ICL8038 276-2334

TEST CIRCUIT

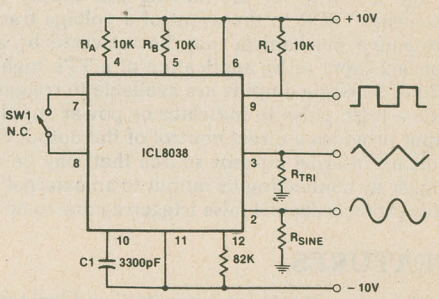
Selecting R_A, R_B AND C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R1 \times V_{SUPPLY}}{(R1 + R2)} \times \frac{1}{R_A} = \frac{V_{SUPPLY}}{5R_A}$$

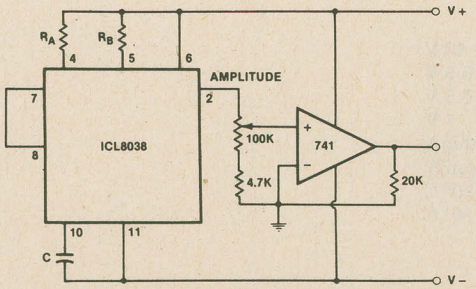
A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.



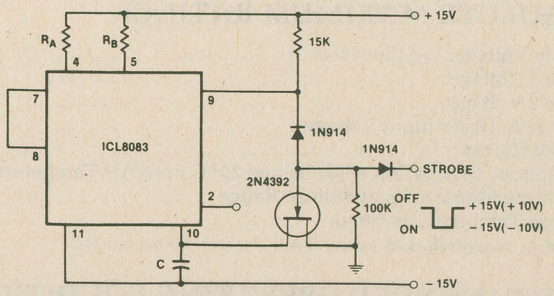
Test Circuit

TYPICAL APPLICATIONS



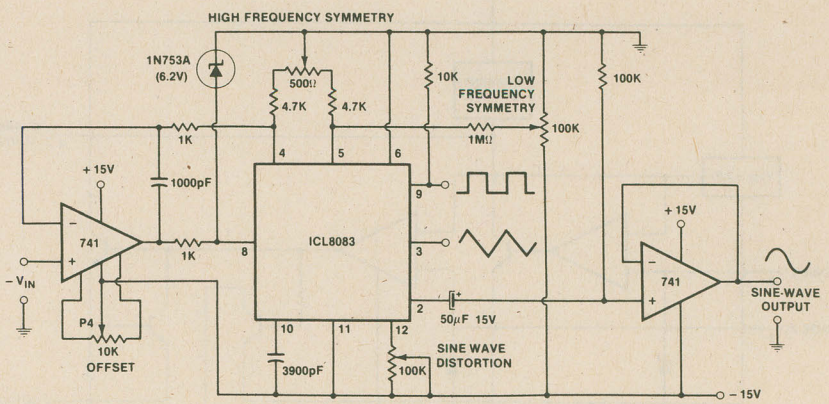
The sine wave output has a relatively high output impedance (1kΩ typical). This circuit provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

Sine Wave Output Buffer Amplifier



With a dual supply voltage the external capacitor on pin 10 can be shorted to ground to halt the 8083 oscillation. This application uses a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

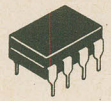
Strobe-Tone Burst Generator



Linear Voltage Controlled Oscillator

MC3423
276-1717

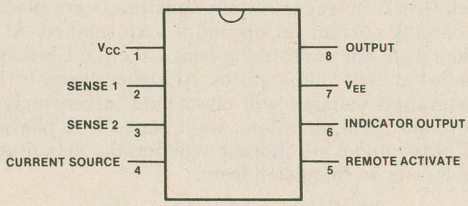
OVERVOLTAGE-SENSING CIRCUIT



GENERAL DESCRIPTION

These overvoltage-sensing circuits are designed to protect sensitive electronic circuitry by monitoring the supply rail and triggering an external "crowbar" SCR in the event of a voltage transient or loss of regulation. The protective mechanism may be activated by an overvoltage condition at the Sense 2 input or by application of a TTL high level to the remote activate terminal. Separate outputs are available to trigger the crowbar circuit and to provide a logic pulse to indicator or power supply control circuitry. The Sense 2 input provides a direct control of the output circuitry. The Sense 1 input controls an internal current source that may be utilized to implement a delayed trigger by connecting its output to an external capacitor and the Sense 2 input. This protects against false triggering due to noise at the Sense 1 input.

PIN CONNECTION



FEATURES

- Separate outputs for "crowbar" and logic circuitry
- Programmable time delay to eliminate noise triggering
- TTL-level activation isolated from voltage-sensing inputs
- 2.6-volt internal voltage reference with temperature coefficient typically 0.08%/°C

ABSOLUTE MAXIMUM RATINGS

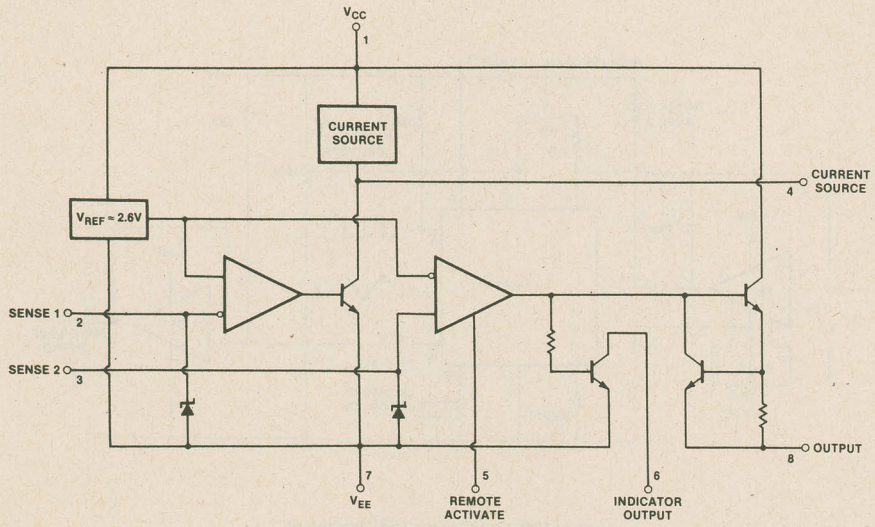
Supply Voltage, V_{CC} (See Note 1) ..... 40 V
Sense 1 Voltage ..... 6.5 V
Sense 2 Voltage ..... 6.5 V
Remote Activate Input Voltage ..... 7 V
Output Current, I_O ..... 300 mA
Continuous Dissipation at (or below) 25°C Free-Air Temperature .... 1000 mW
Operating Free-Air Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... −65 to 150°C

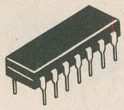
NOTES: 1. Voltage values are measured with respect to the V_{EE} terminal.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply Voltage, V_{CC}	4.5	40	V
High-Level Input Voltage, Remote Activate Input	2		V
Low-Level Input Voltage, Remote Activate Input		0.5	V

BLOCK DIAGRAM





QUAD COMPARATOR

339
276-1712

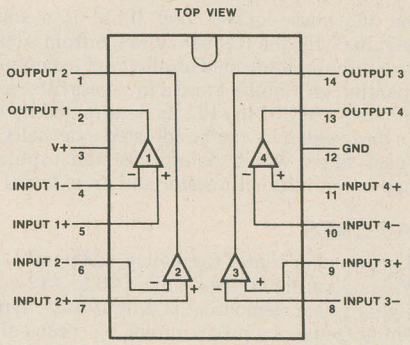
GENERAL DESCRIPTION

The 339 series consists of four independent voltage comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

FEATURES

- Wide single supply:
  Voltage range 2 V_{DC} to 32 V_{DC} or dual supplies ± 1 V_{DC} to ± 16 V_{DC}
- Very low supply current drain (0.8 mA)—independent of supply voltage (1 mW/comparator at +5 V_{DC})
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 1 mV at 5 μA; saturation voltage 70 mV at 1 mA
- Output voltage compatible with TTL (fanout of 2), DTL, ECL, MOS and CMOS logic systems

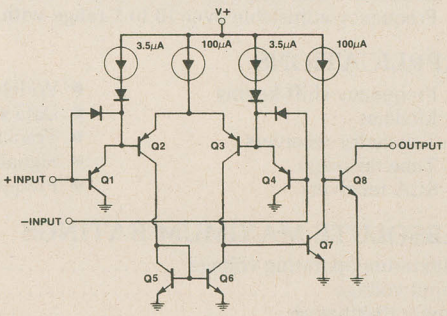
PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

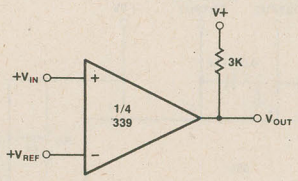
Supply Voltage, V+	32 V_{DC} or ± 16 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation	
Molded DIP	570 mW
Cavity DIP	900 mW
Output Short-Circuit to GND	Continuous
Input Current ($V_{IN} < -0.3$ V_{DC})	50 mA
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

INTERNAL CIRCUIT

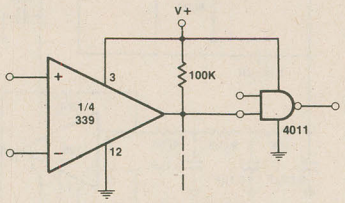


TYPICAL APPLICATIONS

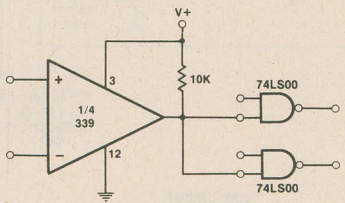
5 VOLT GROUP



Basic Comparator

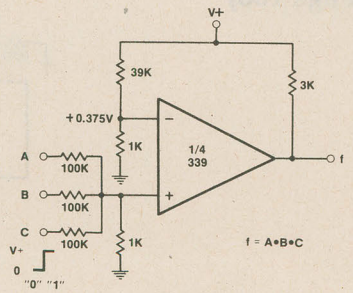


Driving CMOS

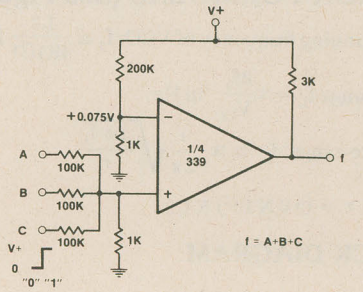


Driving TTL

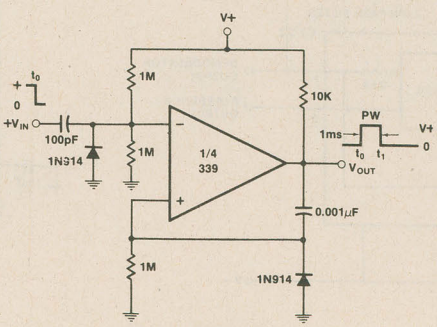
15V GROUP



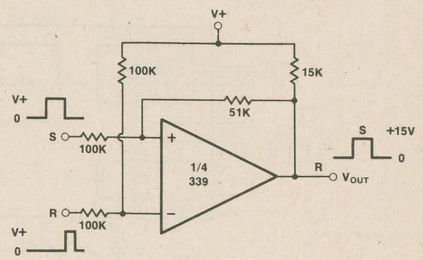
AND Gate



OR Gate



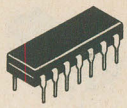
One-Shot Multivibrator



Bi-Stable Multivibrator

565
276-1720

PHASE LOCKED LOOP



GENERAL DESCRIPTION

The 565 phase-locked loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001 Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

- Highly stable center frequency (200ppm/°C typ.)
- Wide operating voltage range (±6 to ±12 volts)
- Highly linear demodulated output (0.2% typ.)
- Center frequency programming by means of a resistor or capacitor, voltage or current
- TTL and LS compatible square-wave output; loop can be opened to insert digital frequency divider.
- Highly linear triangle wave output
- Reference output for connection of comparator in frequency discriminator
- Bandwidth adjustable from < ±1% to > ±60%
- Frequency adjustable over 10 to 1 range with same capacitor

APPLICATIONS

- Frequency shift keying
- Modems
- Telemetry receivers
- Tone decoders
- SCA receivers
- Wideband FM discriminators
- Data synchronizers
- Tracking filters
- Signal restoration
- Frequency multiplication & division

ABSOLUTE MAXIMUM RATINGS

Maximum operating voltage ..... ±12V
Input voltage 3Vp-p
Power dissipation 300mW
Operating temperature range ..... 0 to +70°C
Storage temperature ..... −65 to +150°C

DESIGN FORMULAS (See Figure 1, Page 100)

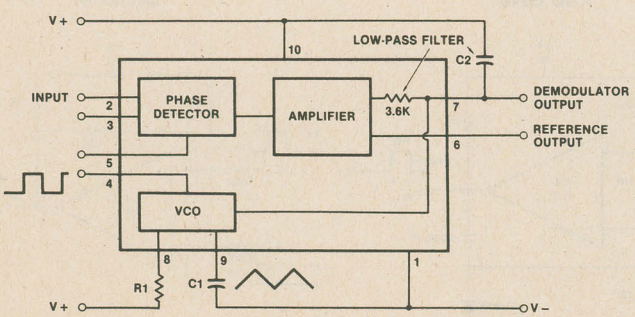
Free-running frequency of VCO: $f_o \cong \frac{1.2}{4R1C1}$ in Hz

Lock-range $f_L = \pm\frac{8f_o}{V_{CC}}$ in Hz

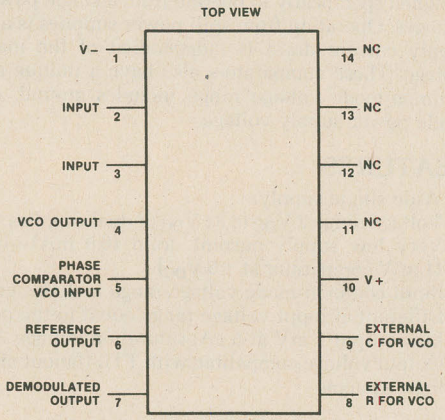
Capture-range: $f_C \cong \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C2$

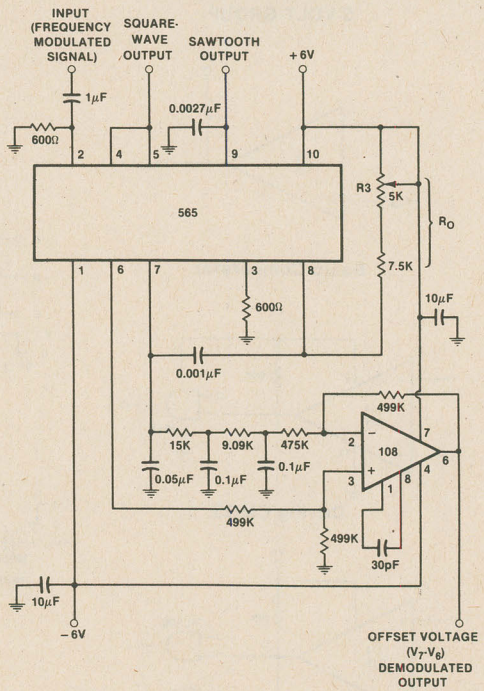
BLOCK DIAGRAM



PIN CONNECTION



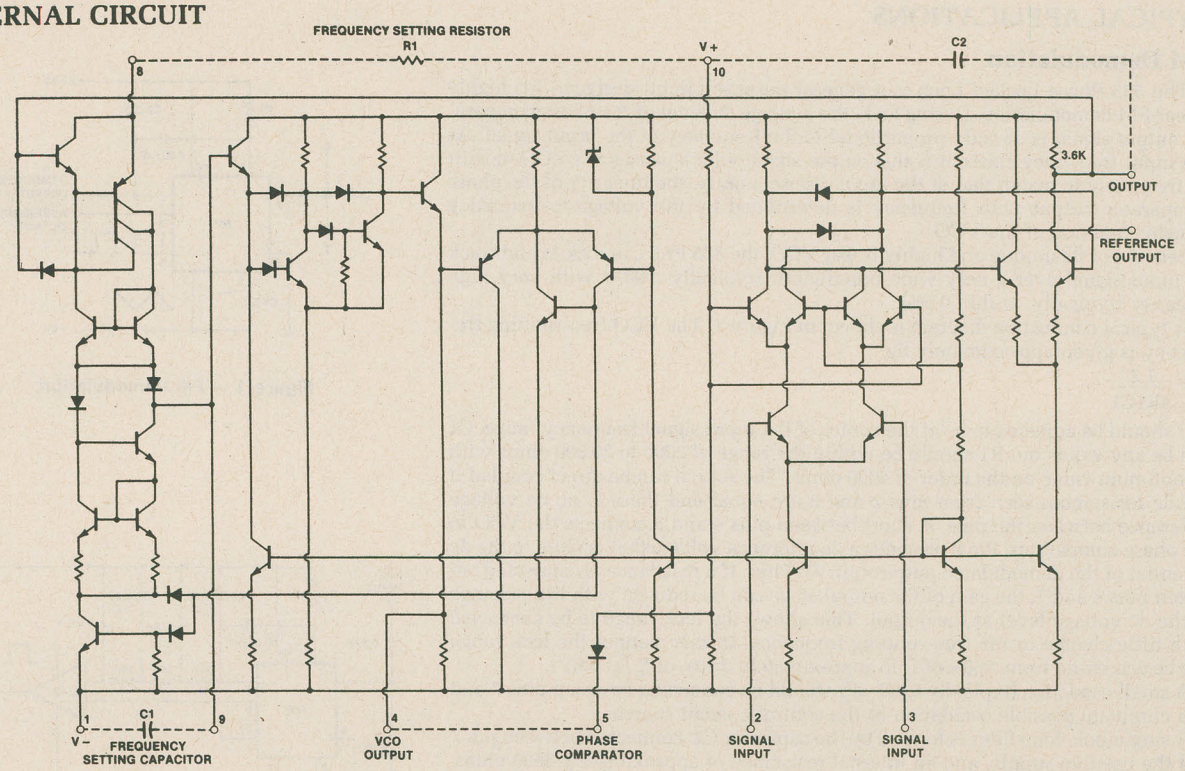
TEST CIRCUIT



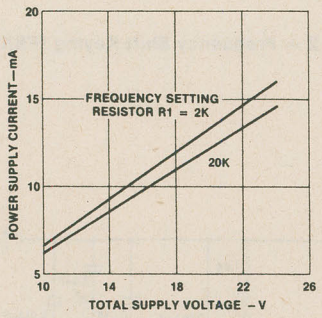
Test Circuit

565 276-1720

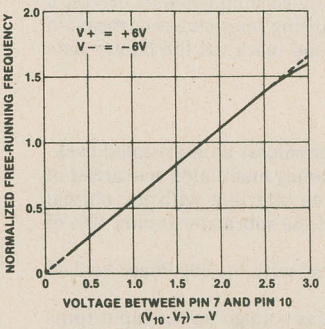
INTERNAL CIRCUIT



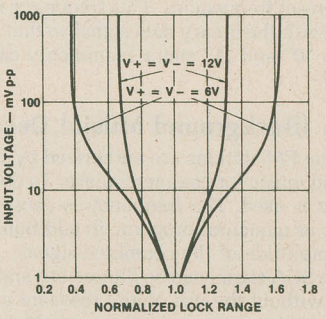
TYPICAL CHARACTERISTICS



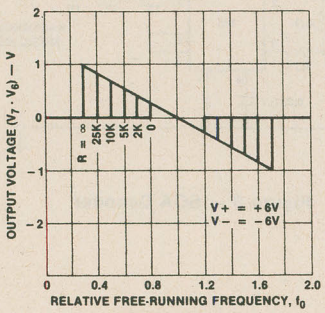
Power Supply Current vs Total Supply Voltage



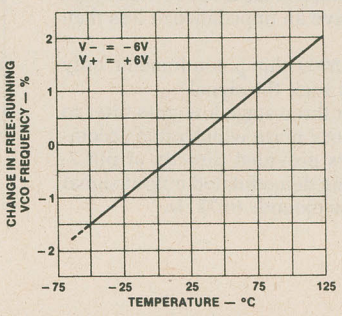
Normalized Free Running Frequency vs Voltage Between Pin 7 and Pin 10



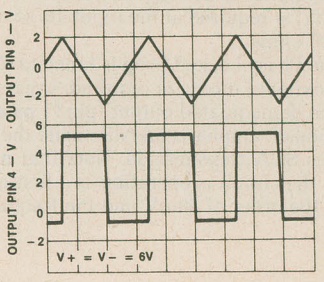
Input Voltage vs Normalized Lock Range



Output Voltage vs Relative Free Running Frequency



Change in Free-Running VCO Frequency vs Temperature



VCO Output Waveform

565 276-1720

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide brandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$$f_o = \frac{1.2}{4R1C1}$$

and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_o to approximately ±20% of f_o (at ±6V).

A small capacitor (typically 0.001 μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

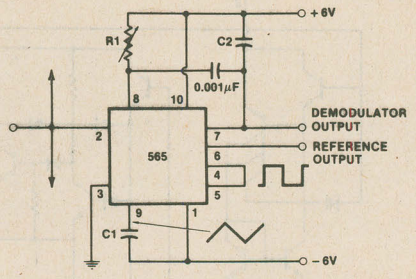


Figure 1 — FM Demodulation

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

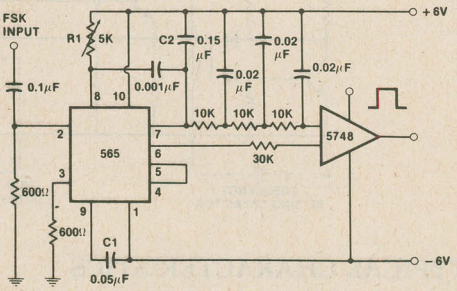


Figure 2 — Frequency Shift Keying (FSK)

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the 565 Phase Locked Loop without the use of any resonant circuits.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer, only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

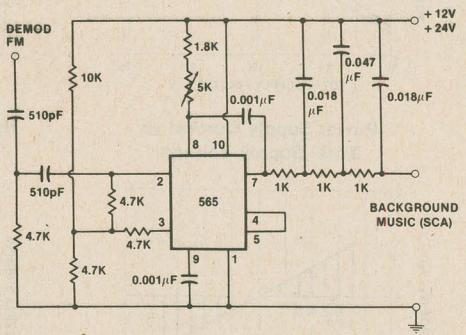


Figure 3 — SCA Decoder

TONE DECODER

567
276-1721

GENERAL DESCRIPTION

The 567 is a general purpose tone decoder designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

FEATURES

- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

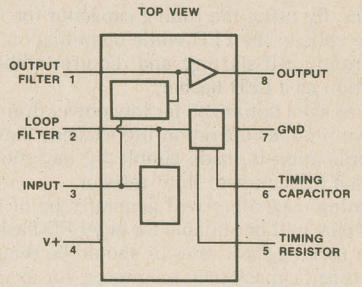
APPLICATIONS

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

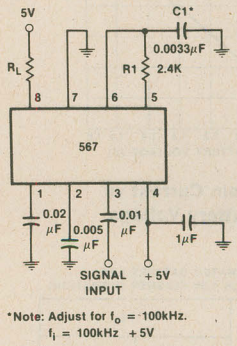
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	9V
Power Dissipation	300 mW
V_8 (Output Voltage)	15V
V_3 (−Voltage at Input)	−10V
V_3 (+Voltage at Input)	V_8 +0.5V
Operating Temperature	0 to +70°C
Storage Temperature Range	−65 to +150°C

PIN CONNECTION



TYPICAL APPLICATIONS



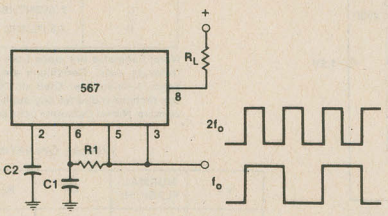
*Note: Adjust for f_o = 100kHz.
f_i = 100kHz +5V

The center frequency of the tone decoder is equal to the free-running frequency of the VCO.
This is given by $f_o \cong 1/R1C1$
The band width of the filter may be found from the approximation

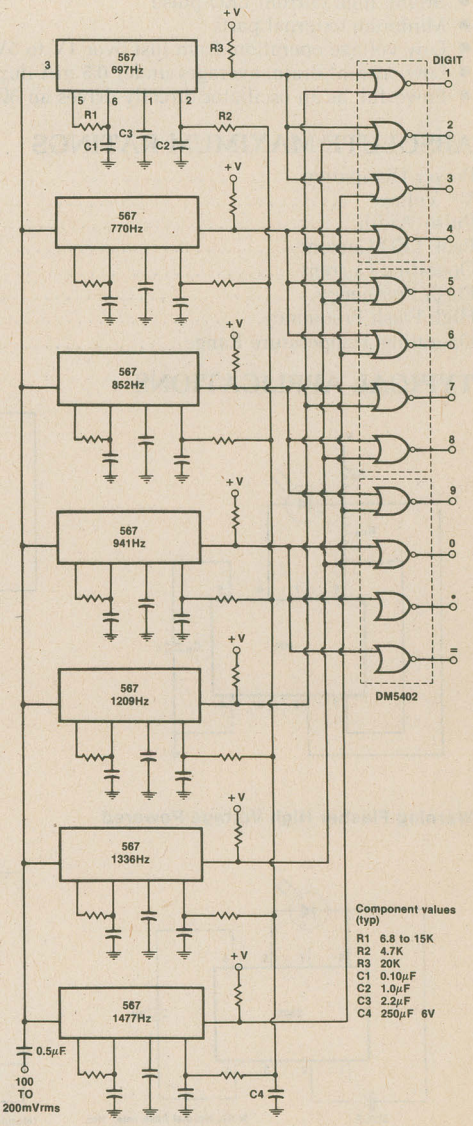
$$BW = 1070 \sqrt{\frac{V_{IN}}{f_o C2}} \text{ in \% of } f_o.$$

Where: V_{IN} = Input voltage (volts rms), $V_{IN} \leq 200mV$.
C2 = Capacitance at pin 2 in μF.

AC Test Circuit



Oscillator with Double Frequency Output



Touch-Tone Decoder

3909
276-1705

LED FLASHER/OSCILLATOR

GENERAL DESCRIPTION

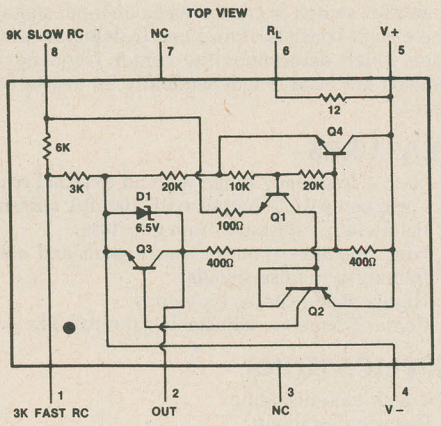
The 3909 is a monolithic oscillator specifically designed to flash light emitting diodes. By using the timing capacitor for voltage boost, it delivers pulses of 2 or more volts to the LED while operating on a supply of 1.5V or less. The circuit is inherently self-starting, and requires addition of only a battery and capacitor to function as a LED flasher.

It has been optimized for low power drain and operation from weak batteries so that continuous operation life exceeds that expected from battery rating.

Application is made simple by inclusion of internal timing resistors and an internal LED current limit resistor.

Timing capacitors will generally be of the electrolytic type, and a small 3V rated part will be suitable for any LED flasher using a supply up to 6V. However, when picking flash rates, it should be remembered that some electrolytics have very broad capacitance tolerances, for example −20% to +100%.

PIN CONNECTION



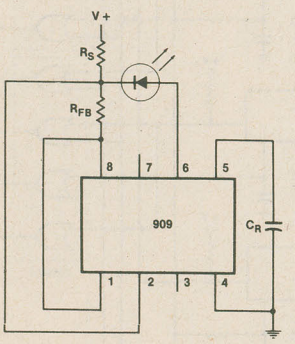
FEATURES

- Operation over one year from one C size flashlight cell
- Bright, high current LED pulse
- Minimum external parts
- Low voltage operation, from just over 1V to 5V
- Low current drain, averages under 0.5 mA during battery life
- Powerful; as an oscillator directly drives an 8Ω speaker

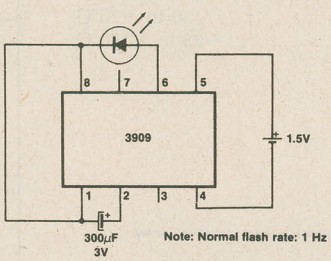
ABSOLUTE MAXIMUM RATINGS

Power Dissipation	500 mW
V+ Voltage	6.4V
Pulse Width	6 ms
Peak LED Current	45 mA
Operating Current	75 mA
Flash Frequency	1.3 Hz
High Flash Frequency	1.1 kHz
Operating Temperature Range	−25 to +70°C

TYPICAL APPLICATIONS

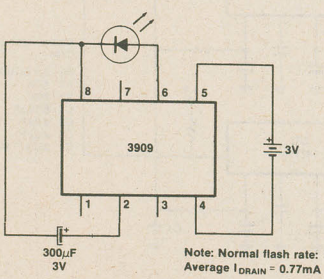


Warning Flasher High Voltage Powered



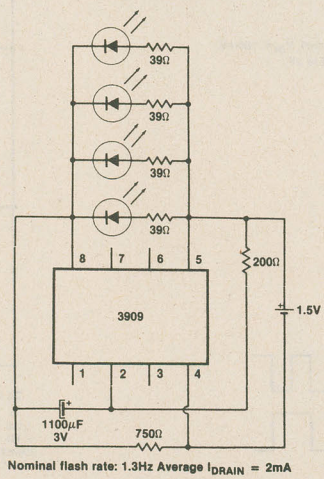
Note: Normal flash rate: 1 Hz

1.5V Flasher



Note: Normal flash rate: 1Hz.
Average I_{DRAIN} = 0.77mA

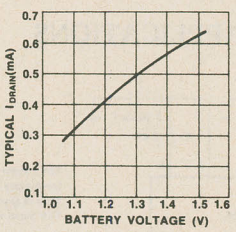
3V Flasher



Nominal flash rate: 1.3Hz Average I_{DRAIN} = 2mA

Parallel LED's

TYPICAL CHARACTERISTICS



Drain Current vs Battery Voltage

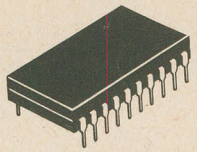
ESTIMATED BATTERY LIFE
(CONTINUOUS 1.5V FLASHER OPERATION)

SIZE CELL	TYPE	
	STANDARD	ALKALINE
AA	3 MONTHS	6 MONTHS
C	7 MONTHS	15 MONTHS
D	1.3 YEARS	2.6 YEARS

Note: Estimates are made from our tests and manufacturers data. Conditions are fresh batteries and room temperature. Clad or "leak-proof" batteries are recommended for any application of five months or more. Nickel Cadmium cells are not recommended.

TYPICAL OPERATING CONDITIONS

V+	NORMAL FLASH Hz	C_T	R_S 1W	R_{FB}	$V+_{RANGE}$
6V	2	400μF	1K	1.5K	5-25V
15V	2	180μF	3.9K	1K	13-50V
100V	1.7	180μF	43K	1K	85-200V



8-BIT MICROPROCESSOR COMPATIBLE A/D CONVERTER

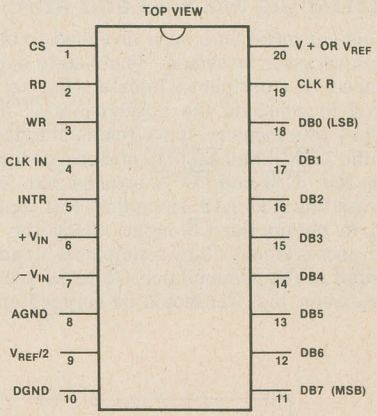
ADC0801
276-1792

GENERAL DESCRIPTION

The ADC0801 is a CMOS 8-bit successive approximation A/D converter which uses a modified potentiometric ladder, and is designed to operate with the 8080A control bus via three-state outputs. This converter appears to the processor as memory locations or I/O ports, hence no interfacing logic is required.

The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

PIN CONNECTION



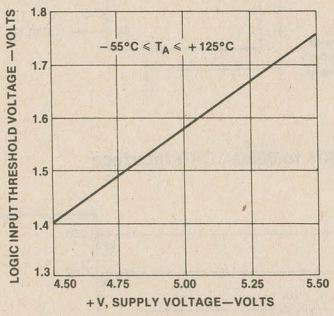
FEATURES

- MCS-48 and MCS-80/85 bus compatible — no interfacing logic required
- Conversion time<100μs
- Easy interface to all microprocessors
- Will operate "stand alone"
- Differential analog voltage inputs
- Works with bandgap voltage references
- TTL compatible inputs and outputs
- On-chip clock generator
- 0 to 5 V analog voltage input range (single +5 V supply)
- No zero-adjust required

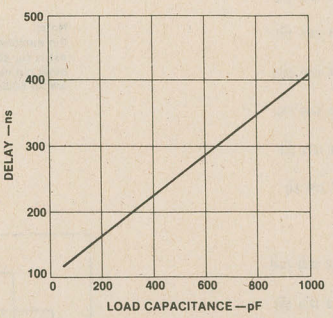
ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . 6.5 V
Voltage at Any Input . . . . . −0.3 to +0.3 V
Storage Temperature Range . . . . . −65 to +150°C
Package Dissipation at T_A = +25°C . . . . . 875 mW
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

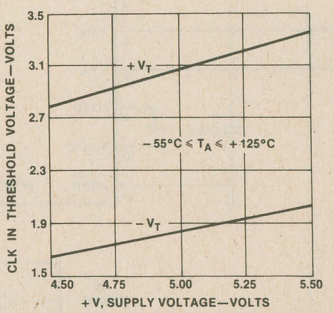
TYPICAL CHARACTERISTICS



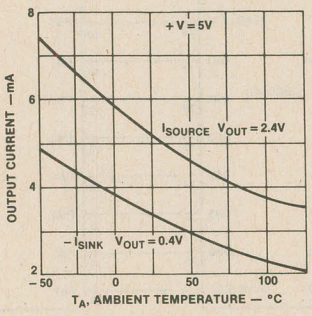
Logic Input Threshold Voltage vs Supply Voltage



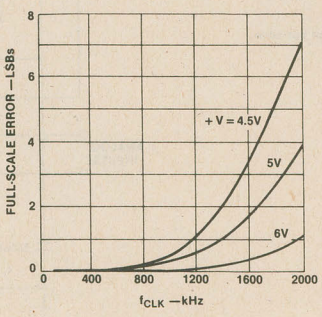
Delay from Falling Edge of RD to Output Data Valid vs Load Capacitance



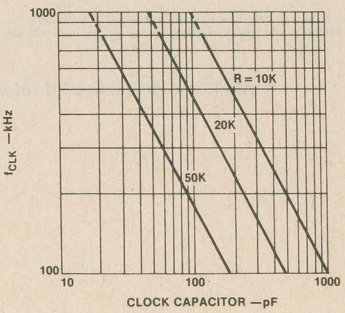
CLK IN Schmitt Trip Levels vs Supply Voltage



Output Current vs Ambient Temperature



Full-Scale Error vs Clock Frequency



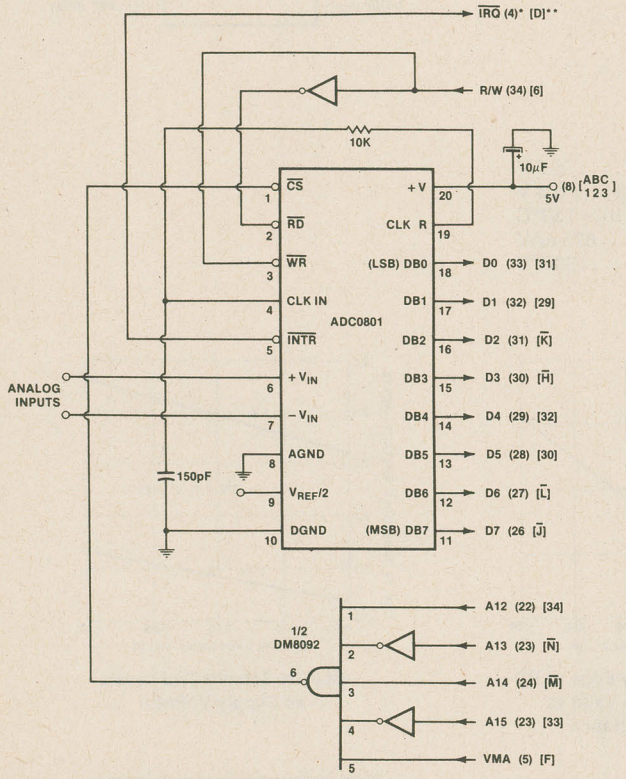
Clock Frequency vs Clock Capacitor

ADC0801 276-1792

TYPICAL APPLICATIONS

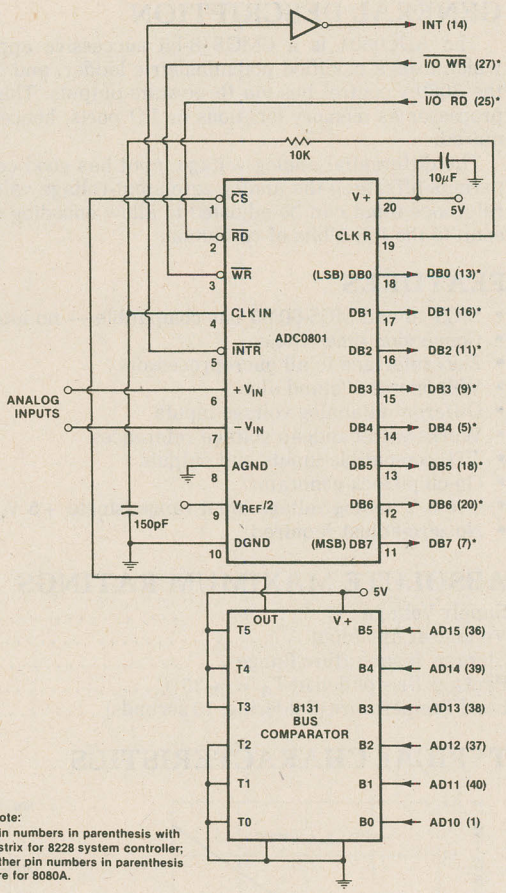
Interfacing MCS-48 and MSC-80/85 Processors

This converter has been designed to directly interface with an MCS-80/85 microprocessor or system. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 - A7 (or address bits A8 - A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space.



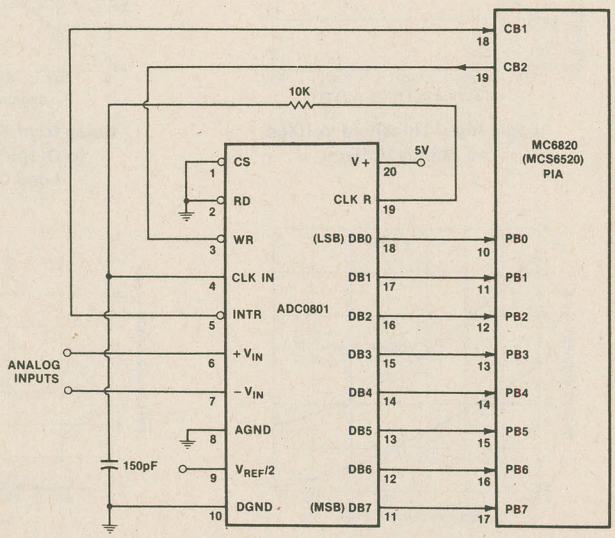
*Note: Numbers in parenthesis refer to MC6800 CPU pin out.
** Note: Numbers and letters in brackets refer to standard MC6800 system common bus code.

ADC0801 to MC6800 CPU Interface



Note:
Pin numbers in parenthesis with astrix for 8228 system controller; other pin numbers in parenthesis are for 8080A.

ADC0801 to 8080A CPU Interface



ADC0801 to MC6820 PIA Interface

LOW VOLTAGE REFERENCE

ICL8069
276-1793

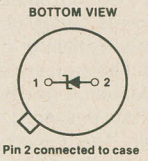
GENERAL DESCRIPTION

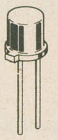
The ICL8069 is a 1.2 V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50 μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

FEATURES

- Temperature coefficients guaranteed to 10 ppm/°C max.
- Low bias current . . . 50 μA min
- Low dynamic impedance
- Low reverse voltage
- Low cost

PIN CONNECTION





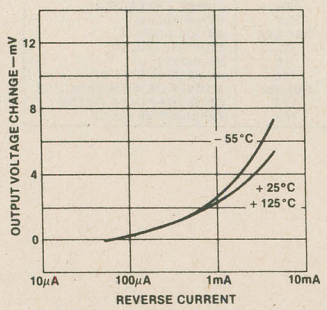
ABSOLUTE MAXIMUM RATINGS

Reverse Voltage (See Note 1) . . . . . 1.25 V
Forward Current . . . . . 10 mA
Reverse Current . . . . . 10 mA
Power Dissipation . . . . . Limited by max forward/reverse current
Storage Temperature . . . . . – 65 to + 200°C
Operating Temperature . . . . . 0 to + 70°C

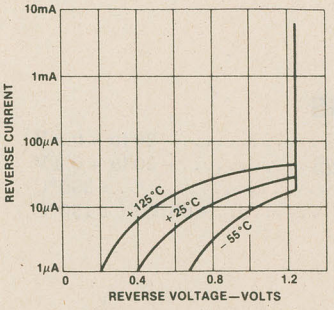
(1) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20 V.

(2) The diode should not be operated with shunt capacitances between 200pF and 0.22 μF, as it may oscillate at some currents. If circuit strays in excess of 200pF are anticipated, a 4.7 μF shunt capacitor will ensure stability under all operating conditions.

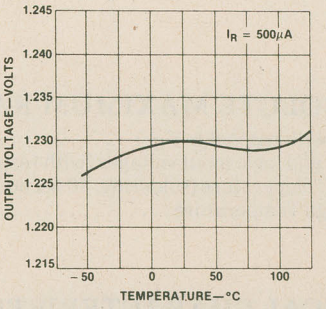
TYPICAL CHARACTERISTICS



Output Voltage Change vs Reverse Current

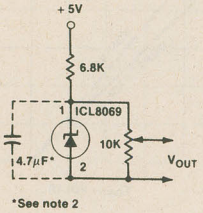


Reverse Current vs Reverse Voltage

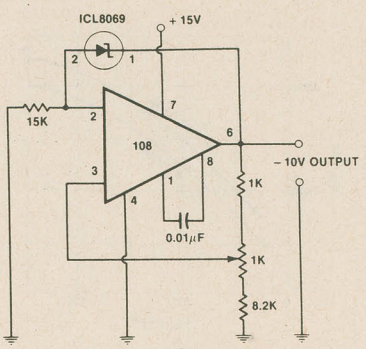


Output Voltage vs Temperature

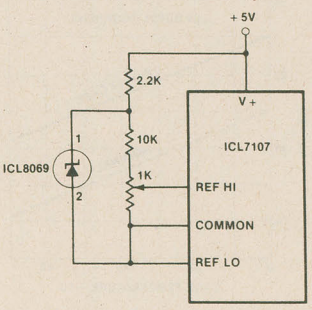
TYPICAL APPLICATIONS



Simple Reference (1.2 volts or less)



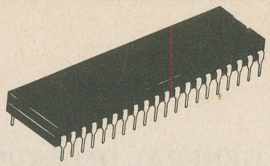
Buffered 10 V Reference Using a Single Supply



Double Regulated 100 mV Reference for ICL7107 One-Chip DPM Circuit

AY-3-1015
276-1794

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER



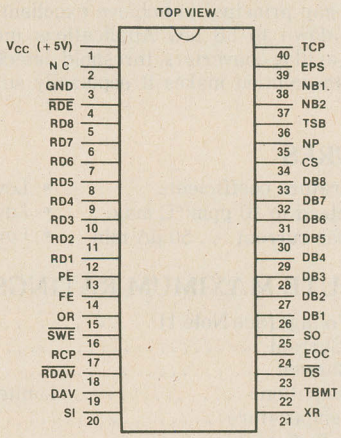
GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

FEATURES

- DTL and TTL compatible — no interfacing circuits required — drives one TTL load
- Fully Double Buffered — eliminates need for system synchronization, facilitates high-speed operation
- Full Duplex Operation — can handle multiple bauds (receiving-transmitting) simultaneously
- Start Bit Verification — decreases error rate with center sampling
- Receiver center sampling of serial input; 48% distortion immunity
- High Speed Operation
- Three-State Outputs — bus structure capability
- Low Power — minimum power requirements
- Input Protected — eliminates handling problems
- GIANT P-channel nitride process
- 0 to 40kbaud
- Pull up resistors to V_{CC} on all inputs

PIN CONNECTION

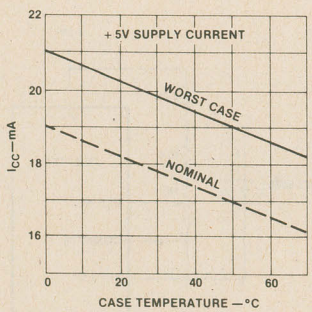


PIN	ABREVIATION	DESCRIPTION
1	V_{CC}	POWER SUPPLY
2	N C	
3	GND	GROUND
4	RDE	RECEIVED DATA ENABLE
5-12	RD8-RD1	RECEIVED DATA BITS
13	PE	PARITY ERROR
14	FE	FRAMING ERROR
15	OR	OVER-RUN
16	SWE	STATUS WORD ENABLE
17	RCP	RECEIVER CLOCK
18	RDAV	RESET DATA AVAILABLE
19	DAV	DATA AVAILABLE
20	SI	SERIAL INPUT
21	XR	EXTERNAL RESET
22	TBMT	TRANSMITTER BUFFER EMPTY
23	DS	DATA STROBE
24	EOC	END OF CHARACTER
25	SO	SERIAL OUTPUT
26-33	DB1-DB8	DATA BIT INPUTS
34	CS	CONTROL STROBE
35	NP	NO PARITY
36	TSB	NUMBER OF STOP BITS
37-38	NB2,NB1	NUMBER OF BITS/CHARACTER
39	EPS	ODD/EVEN PARITY SELECT
40	TCP	TRANSMITTER CLOCK

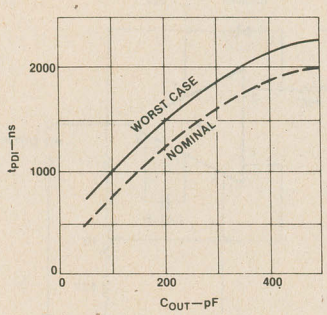
ABSOLUTE MAXIMUM RATINGS

V_{GG} (with respect to V_{CC}) ..... − 20 to + 0.3 V
Clock and logic input voltages (with respect to V_{CC}) ..... − 20 to + 0.3 V
Lead Temperature (soldering, 10 seconds) ..... + 330°C
Storage Temperature ..... − 65°C to + 150°C

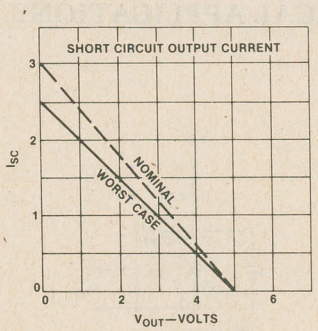
TYPICAL CHARACTERISTICS



5 V Supply Current vs Case Temperature



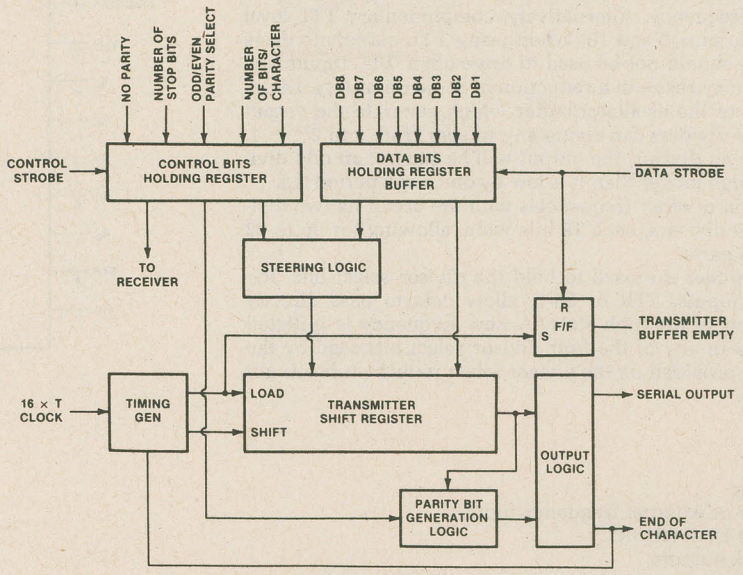
Delay Time vs Output Capacitance



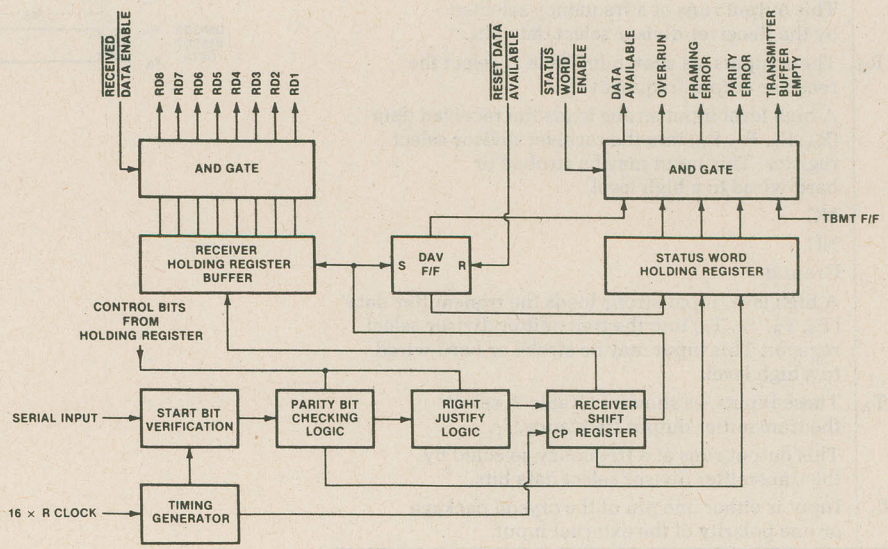
Short Circuit Output Current vs Output Voltage

AY-3-1015 276-1794

TRANSMITTER BLOCK DIAGRAM

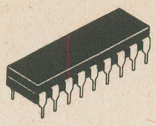


RECEIVER BLOCK DIAGRAM



AY-5-8116 DUAL BAUD RATE GENERATOR

276-1795



GENERAL DESCRIPTION

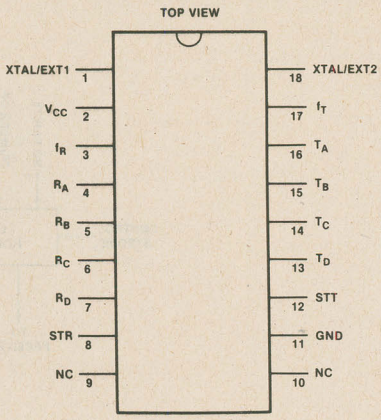
The AY-5-8116 is a very versatile Dual Buad Rate Generator.

This device is designed to generate the full spectrum of 16 asynchronous/synchronous date communication frequencies for use with 16× UART/USRT devices. An on-chip crystal oscillator available on the 8116 is capable of providing a master reference frequency. Alternatively, complimentary TTL level clock signals can be input to pins 1 and 18. When using TTL outputs to drive the XTAL/EXT inputs, they should not be used to drive other TTL inputs due to excessive loading which may result in a reduction of noise immunity. Dividers are used on the output of the oscillator/buffer which generate the output frequencies f_T and f_R. These dividers can divide any integer from 6 to $2^{19} + 1$, inclusive. When using an even divisor, the output will be square; an odd divisor will cause output to be high longer than it is low by one clock period (f_x).

The 8116 allows generation of other frequencies with the use of its two divisor ROMs which contain 16 divisors, each 19 bits wide, allowing for up to 32 different divisors on custom parts.

Externally strobed data latches are used to hold the divisor select bits, R_A-R_D and T_A-T_D. The strobe inputs, STR or STT, allow data to pass directly through the data latch when in the high state. A new frequency is initiated within 3.5 μsec of a change in any of the four divisor select bits read by the device. Pull-up resistors are provided on the divisor select inputs while are not present on the strobe inputs.

PIN CONNECTION



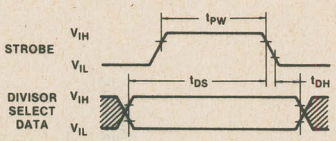
FEATURES

- Single +5V power supply
- On-chip crystal oscillator or external frequency input
- Direct compatibility with UART/USRT
- Dual selectable 16× clock outputs
- Reprogrammable ROM allowing generation of non-standard frequencies
- TTL, MOS compatibility

PIN FUNCTIONS

Pin. No.	Signal	Function
1	XTAL/EXT1	Input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Positive power supply—normally +5V.
3	f_R	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	These inputs, as shown in Table 1, select the receiver output frequency f_R.
8	STR	A high level input strobe loads the received data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	NC
10	NC	NC
11	GND	Ground
12	STT	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobe or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	These inputs, as shown in Table 1, select the transmitter output frequency, f_T.
17	f_T	This output runs at a frequency selected by the transmitter divisor select data bits.
18	XTAL/EXT$_2$	Input is either one pin of the crystal package or one polarity of the external input.

TIMING DIAGRAM



AY-5-8116 276-1795

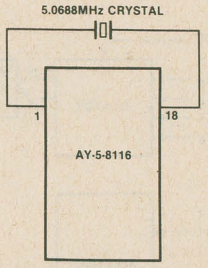
ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with Respect to Ground ..... +8.0V
Negative Voltage on any Pin, with Respect to Ground ..... −0.3V
Power Supply Current, I_{CC} 50mA
Operating Temperature Range ..... 0 to +70°C
Storage Temperature Range ..... −55 to +150°C

AC CHARACTERISTICS

Clock Frequency, f_x (XTAL/EXT, 50% Duty Cycle ±5%) ..... 5.1 MHz
Strobe Pulse Width, t_{PW} ..... 150 ns
Input Set-up Time, t_{DS} ..... 200 ns
Input Hold Time, t_{DH} ..... 50 ns
Strobe to new Frequency Delay (@f_x = 5.0 MHz) ..... 3.5 μs

CRYSTAL OPERATION



Crystal Operation

TABLE 1

REFERENCE FREQUENCY = 5.068800MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (kHz)	Divisor	Actual Baud Rate	Actual Frequency (kHz)	Deviation
0000	50.00	16×	0.80000	6336	50.00	0.800000	0.0000%
0001	75.00	16×	1.20000	4224	75.00	1.200000	0.0000%
0010	110.00	16×	1.76000	2880	110.00	1.760000	0.0000%
0011	134.50	16×	2.15200	2355	134.52	2.152357	0.0166%
0100	150.00	16×	2.40000	2112	150.00	2.400000	0.0000%
0101	300.00	16×	4.80000	1058	300.00	4.800000	0.0000%
0110	600.00	16×	9.60000	528	600.00	9.600000	0.0000%
0111	1200.00	16×	19.20000	264	1200.00	19.200000	0.0000%
1000	1800.00	16×	28.80000	176	1800.00	28.800000	0.0000%
1001	2000.00	16×	32.00000	158	2005.06	32.081013	0.2532%
1010	2400.00	16×	38.40000	132	2400.00	38.400000	0.0000%
1011	3600.00	16×	57.60000	88	3600.00	57.600000	0.0000%
1100	4800.00	16×	76.80000	66	4800.00	76.800000	0.0000%
1101	7200.00	16×	115.20000	44	7200.00	115.200000	0.0000%
1110	9600.00	16×	153.60000	33	9600.00	153.600000	0.0000%
1111	19200.00	16×	307.20000	16	19800.00	316.800000	3.1250%

REFERENCE FREQUENCY = 4.915200MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (kHz)	Divisor	Actual Baud Rate	Actual Frequency (kHz)	Deviation
0000	50.00	16×	0.80000	6144	50.00	0.800000	0.0000%
0001	75.00	16×	1.20000	4096	75.00	1.200000	0.0000%
0010	110.00	16×	1.76000	2793	109.93	1.758983	0.0100%
0011	134.50	16×	2.15200	2284	134.50	2.152000	0.0000%
0100	150.00	16×	2.40000	2048	150.00	2.400000	0.0000%
0101	300.00	16×	4.80000	1024	300.00	4.800000	0.0000%
0110	600.00	16×	9.60000	512	600.00	9.600000	0.0000%
0111	1200.00	16×	19.20000	256	1200.00	19.200000	0.0000%
1000	1800.00	16×	28.80000	171	1796.49	28.743859	0.1949%
1001	2000.00	16×	32.00000	154	1994.81	31.916883	0.2597%
1010	2400.00	16×	38.40000	128	2400.00	32.000000	0.0000%
1011	3600.00	16×	57.60000	85	3614.11	57.825882	0.3921%
1100	4800.00	16×	76.80000	64	4800.00	76.800000	0.0000%
1101	7200.00	16×	115.20000	43	7144.19	114.306976	0.7751%
1110	9600.00	16×	153.60000	32	9600.00	153.600000	0.0000%
1111	19200.00	16×	307.20000	16	19200.00	307.200000	0.0000%

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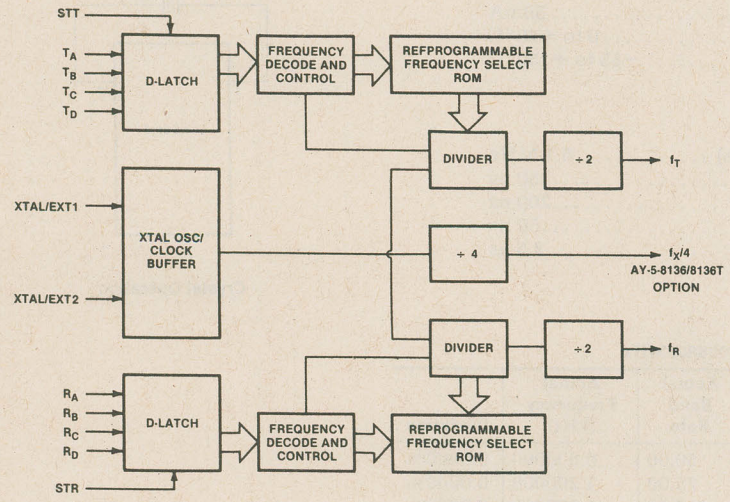
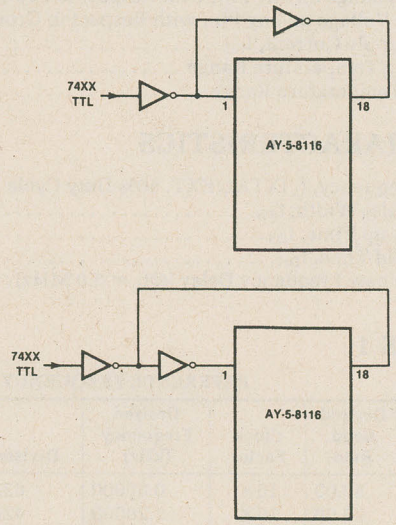
BLOCK DIAGRAM



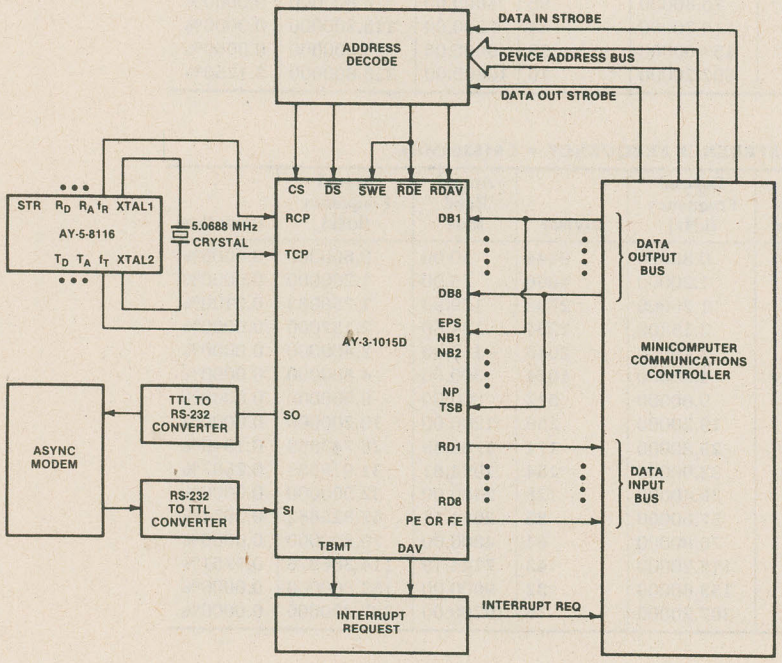
EXTERNAL INPUT OPERATION



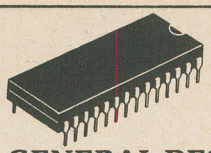
74XX-totem pole or open collector output (external pull-up resistor required)

External Input Operation

TYPICAL APPLICATION



Minicomputer Interface
AY-3-1015D UAR/T + AY-5-8116
Dual Baud Rate Generator



TUNES SYNTHESIZER AY-3-1350

276-1782

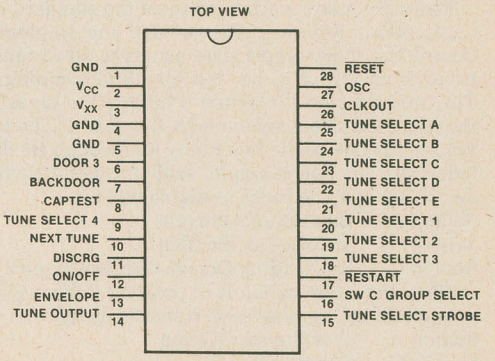
GENERAL DESCRIPTION

The AY-3-1350 is an N-channel MOS microcomputer based synthesizer of pre-programmed tunes for applications in toys, musical boxes, and doorchimes. The standard device has a set of 25 different popular and classical tunes chosen for their international acceptance. In addition there are 3 chimes making a total of 28 tunes.

The chip is mask-programmable during manufacture enabling the quantity user to select his own music. Up to 28 tunes of varying length can be chosen.

The device has multi-mode operation making it suitable for a wide variety of applications.

PIN CONNECTION



FEATURES

- 25 different tunes plus 3 chimes
- Mask programmable with customer specified tunes for toys, musical boxes, etc.
- Minimal external components
- Automatic switch-off signal at end of tune for power savings
- Envelope control to give organ or piano quality
- Sequential tune mode
- 4 door capability when used as doorchime
- Operation with tunes in external PROM if required
- Single supply (+5V) operation

TUNES

The standard AY-3-1350 contains the following tunes:

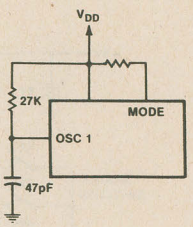
A0	Toreador	A3	O Sole Mio
B0	William Tell	B3	Santa Lucia
C0	Hallelujah Chorus	C3	The End
D0	Star Spangled Banner	D3	Blue Danube
E0	Yankee Doodle	E3	Brahms' Lullaby
A1	John Brown's Body	A4	Hell's Bells
B1	Clementine	B4	Jingle Bells
C1	God Save the Queen	C4	La Vie en Rose
D1	Colonel Bogey	D4	Star Wars
E1	Marseillaise	E4	Beethoven's 9th
A2	America, America		
B2	Deutschland Leid		
C2	Wedding March		Chime X Westminster Chime
D2	Beethoven's 5th		Chime Y Simple Chime
E2	Augustine		Chime Z Descending Octave Chime

ABSOLUTE MAXIMUM RATINGS

Primary Supply Voltage, V_{DD} 7V
Output Buffer Supply Voltage, V_{XX} 9V
Primary Supply Current (No Load), I_{DO} 55mA
Output Buffer Supply Current (No Load), I_{XX} 5mA
Logic Input Low Voltage, V_{IL} 0.8V
Logic Input High Voltage (Note 2), V_{IH1} ..... V_{DD}V
(Except $\overline{\text{RESET}}$ and OSC when driven externally)
Logic Input High Voltage, V_{IH2} ..... V_{DD}V
($\overline{\text{RESET}}$ and OSC)
Logic Output High Voltage (Note 2), V_{OH}(I_{OH} = 100μA) 2.4V
Logic Output Low Voltage, V_{OL} (I_{OL} = 1.6μA, V_{XX} = 4.5V) 0.45V
(I_{OL} = 5mA, V_{XX} = 9V) 0.90V
(I_{OL} = 5mA, V_{XX} = 9V) 0.50V
(I_{OL} = 10mA, V_{XX} = 9V) (Note 1) 0.90V
Operating Temperature ..... 0 to 70°C

Notes: 1. Total I_{OL} for all registers must be less than 150mA under any conditions.
2. Except following pins which have open drain outputs/inputs: 6, 7, 8, 12 and 13.

TEST CIRCUIT



Test Circuit

AY-3-1350 276-1782

TYPICAL APPLICATIONS

Implementation

There are many ways to connect the standard device depending on the exact application. Figure 1 shows just one implementation of the device in a doorchime. This circuit gives access to all 25 tunes from switch A and one of 5 tunes from switch C as well as the descending active chime from switch B. The tune selected for switch B follows the tunes list according to the setting of the two tune select switches (A-E and 0-4). The tune selected from switch C in Figure 1 is one of the five tunes A0 through E0 depending on the setting of the letter switch. For example, with the letter switch set at E and the number switch set at 4, the tunes available will be:

Switch A: Beethoven's 9th (E4)
Switch C: Yankee Doodle (EO)
Switch B: Descending Octave Chime (Chime Z)

When the letter switch is in position F there will be chimes on all doors independent of the number switch setting as follows:

Switch A: Westminster Chime
Switch C: Simple Chime
Switch B: Descending Octave Chime

There is virtually no power consumption in the standby condition (external transistor leakages only). When any door switch is activated the circuit powers up, plays a tune, and then automatically powers down again to conserve the battery, even if the operator keeps his finger on the switch to the end of the tune. He must release it and re-press to play again with the circuit in Figure 1. Activating any of the door switches will pull point A to ground turning on the PNP transistor in the power supply line. This causes +5V to be applied to the AY-3-1350 and the first operation of the chip is to put ON/OFF (pin 12) to logic 0. This maintains the power through the PNP, even after the switch is released. The device can turn off its own power at the end of a tune by raising ON/OFF to logic 1.

Figure 1 shows only a typical one-chip implementation. Further options come from use of different switching and/or from use of the next tune facilities built into the chip. These will now be considered in turn.

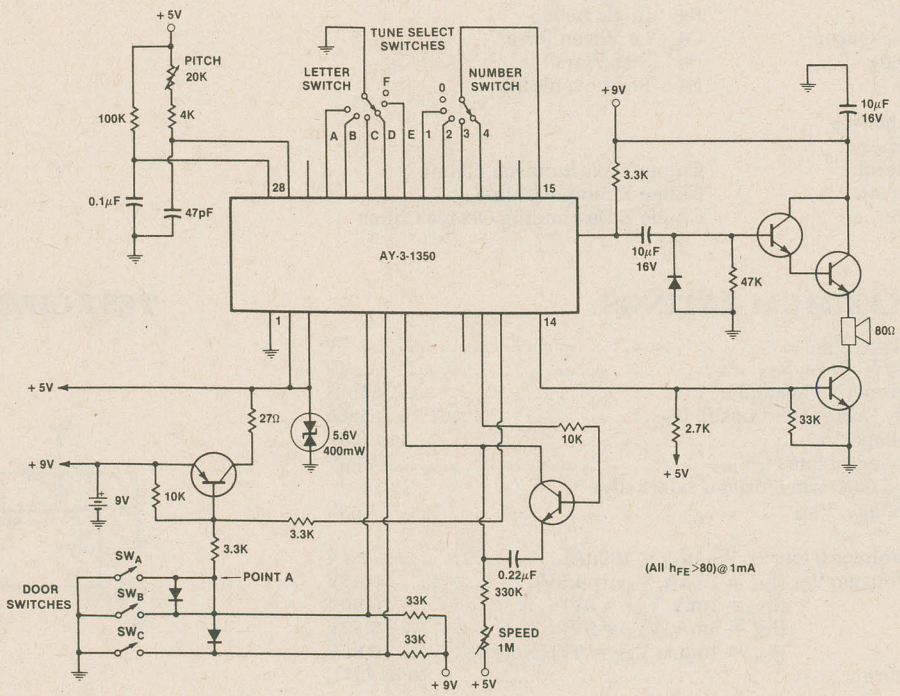


Figure 1—System Diagram

TYPICAL APPLICATIONS (Cont'd)

Switching Options

In Figure 1 the Switch C Group Select pin (16) is not connected, and one of the five tunes (A0 through E0) will play if switch C is activated. Other number groups can be chosen by connecting the Switch C Group Select pin as follows:

Switch C Group Select pin (16) is connected to:	Switch C Tunes
no other pin	A0-E0
Tune Select 1 (pin 20)	A1-E1
Tune Select 2 (pin 19)	A2-E2
Tune Select 3 (pin 18)	A3-E3
Tune Select 4 (pin 9)	A4-E4

Which of the five possible switch C tunes will be played depends on the current setting of the LETTER SWITCH A-E.

Switch C selection can be made by hard-wire connection for a permanent selection or a third switch can be added for an additional group selection feature.

LED Direct Drive

V_{XX} drives the gate of the output buffer, allowing adjustment of drive capability:

V_{XX}	V_{OUT}	I_{SINK} (typ.)
5V	0.4V	2.5mA
5V	0.7V	4.2mA
10V	0.4V	5.8mA
10V	0.7V	10.0mA
10V	1.0V	14.1mA

Using the power-up circuit of Figure 1, the AY-3-1350 will have +5V applied and be latched within a few microseconds (dependant upon external components) from any bell-push closing. The device starts to operate when the RESET pin reaches logic 1 (about 10ms with components shown) but in fact the tune select switches are not interrogated until approximately 6 ms later. The total is sufficient for most bell-pushes to complete any bounce period and for a firm selection of tunes to be made.

Next Tune Facilities

At the end of tune play the circuit of Figure 1 powers down because ON/OFF (pin 12) is raised to a logic 1. This simplified flow diagram in Figure 3 shows that before the power down there is a test for connection between NEXT TUNE (pin 10) then RESTART (pin 17) with TUNESELECT 4 (pin 9). At this time NEXT TUNE (pin 10) then RESTART (pin 17), which is normally at logic 1, output a logic 0. This is looked for at input TUNESELECT 4 (pin 9). If neither is found the power down system is reached as in Figure 1.

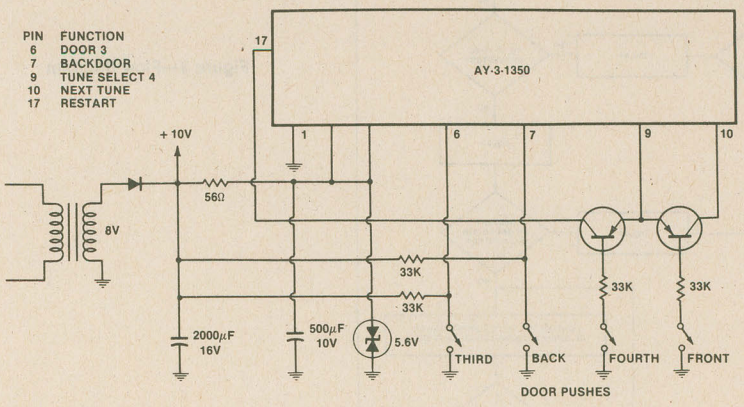


Figure 2

AY-3-1350 276-1782

TYPICAL APPLICATIONS (Cont'd)

A NEXT TUNE (pin 10)—TUNE SELECT 4 (pin 9) connection at the moment of test causes the next tune in the list to be played after a short pause (equal to a musical breve—the actual time depends on the setting of the tune speed control). The order of the tunes is A0 to E4 as given in the listing of standard AY-3-1350 tunes. If the last tune (E4) was played then the circuit will go on to play the first tune A0 (and then successive ones). The chimes are not included in the cycling sequence.

A RESTART (pin 17)—TUNESELECT 4 (pin 9) connection at the moment of test at the end of a tune causes the same selected tune to be played again. Figure 3 shows that in this case the tune sensing mechanism is passed through once more so the tune would be different the second time if the switches were altered while the first tune was playing.

The connections referred to cannot be permanent because otherwise the circuit would never stop playing tunes. Figure 2 shows how transistors are used to make the connection in a practical application.

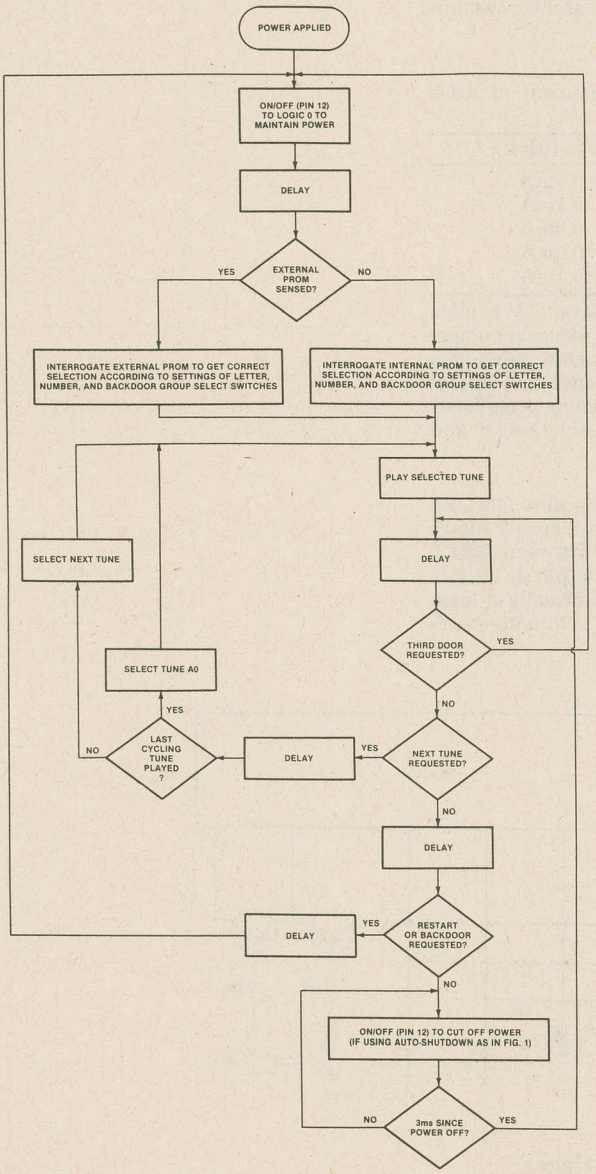
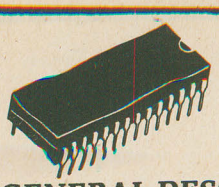


Figure 3—Flow Diagram



SPEECH PROCESSOR SP0256

276-1783

GENERAL DESCRIPTION

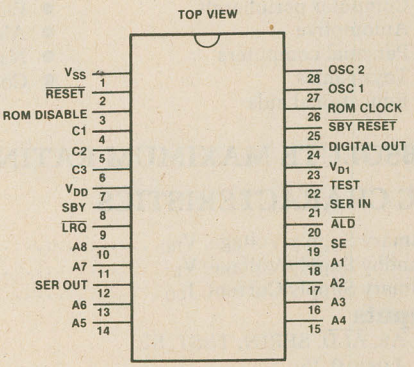
The SP0256 (speech processor) is a single chip N-channel MOS LSI device that is able, using its stored program, to synthesize speech or complex sounds.

The achievable output is equivalent to a flat frequency response ranging from 0 to 5kHz, a dynamic range of 42dB, and a signal to noise ratio of approximately 35dB.

The SP0256 incorporates four basic functions:

1. A software programmable digital filter that can be made to model a VOCAL TRACT.
2. A 16K ROM which stores both data and instructions (THE PROGRAM).
3. A MICROCONTROLLER which controls the data flow from the ROM to the digital filter, the assembly of the "word strings" necessary for linking speech elements together, and the amplitude and pitch information to excite the digital filter.
4. A PULSE WIDTH MODULATOR that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

PIN CONNECTION



FEATURES

- Natural speech
- Stand alone operation with inexpensive support components
- Wide operating voltage
- Word, phrase, or sentence library, ROM expandable
- Expandable to 491K of ROM directly
- Simple interface to most microcomputers or microprocessors
- Supports L.P.C. synthesis: formant synthesis: allophone synthesis

PIN FUNCTIONS

Pin Number	Name	Function
1	V_{SS}	Ground
2	$\overline{\text{RESET}}$	A logic 0 resets the SP. Must be returned to a logic 1 for normal operation.
3	ROM DISABLE	For use with an external serial speech ROM. A logic 1 disables the external ROM.
4,5,6	C1, C2, C3	Output control lines used by an external serial speech ROM.
7	V_{DD}	Primary power supply.
8	SBY	STANDBY. A logic 1 output indicates that the SP is inactive (i.e., not talking) and V_{DD} can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0.
9	$\overline{\text{LRQ}}$	$\overline{\text{LOAD REQUEST}}$. $\overline{\text{LRQ}}$ is a logic 1 output whenever the Input buffer is full. When $\overline{\text{LRQ}}$ goes to a logic 0, the input port is loaded by placing the 8 address bits on A1-A8 and pulsing the $\overline{\text{ALD}}$ Input.
10,11,13,14, 15,16,17,18	A8, A7, A6, A5, A4, A3, A2, A1	8-bit address which defines any one of 256 speech entry points.
12	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM.
19	SE	STROBE ENABLE. Normally held in logic 1 state. When tied to ground, ALD is disabled and the SP will automatically latch in the address on the input bus approximately 1μs after detecting a logic 1 on any address line.
20	$\overline{\text{ALD}}$	$\overline{\text{ADDRESS LOAD}}$. A negative pulse on this input loads the 8 address bits into the input port. The leading edge of this pulse causes $\overline{\text{LRQ}}$ to go high.
21	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22	TEST	A logic 1 places the SP in test mode. This pin should normally be grounded.
23	V_{D1}	Standby power supply for the interface logic and controller.
24	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5kHz low pass filter and amplified, will drive a loudspeaker.
25	$\overline{\text{SBY RESET}}$	$\overline{\text{STANDBY RESET}}$. A logic 0 resets the interface logic. Normally should be a logic 1.
26	ROM CLOCK	1.56MHz clock for an external serial speech ROM.
27	OSC 1	XTAL IN. Input connection for a 3.12 MHz crystal.
28	OSC 2	XTAL OUT. Output connection for a 3.12MHz crystal.

SP0256 276-1783

APPLICATIONS

- Telecommunications
- Appliances
- Computer peripherals
- Automotive
- Personal computers
- Toys/games
- Educational aids
- Warning systems
- Security systems
- Electronic musical instruments
- Aids to the blind
- Narrow bandwidth
- Communication systems

ABSOLUTE MAXIMUM RATINGS

DC CHARACTERISTICS

Primary Supply Voltage, V_{DD} 7V
Standby Supply Voltage, V_{D1} 7V
Primary Supply Current, I_{DD} 90mA

Inputs

A1-A8, $\overline{ALD}$, SERIN, TEST, SE
Logic 0, V_{IL} 0.6V
Logic 1, V_{IH} ..... V_{D1}V
Capacitance, C_{IN} 10pF
Leakage, I_{LC} ..... $\pm 10\mu$A

$\overline{Reset}$, $\overline{SBY\ Reset}$
Logic 0, V_{IL1} 0.6V
Logic 1, V_{IH1} ..... V_{D1}V

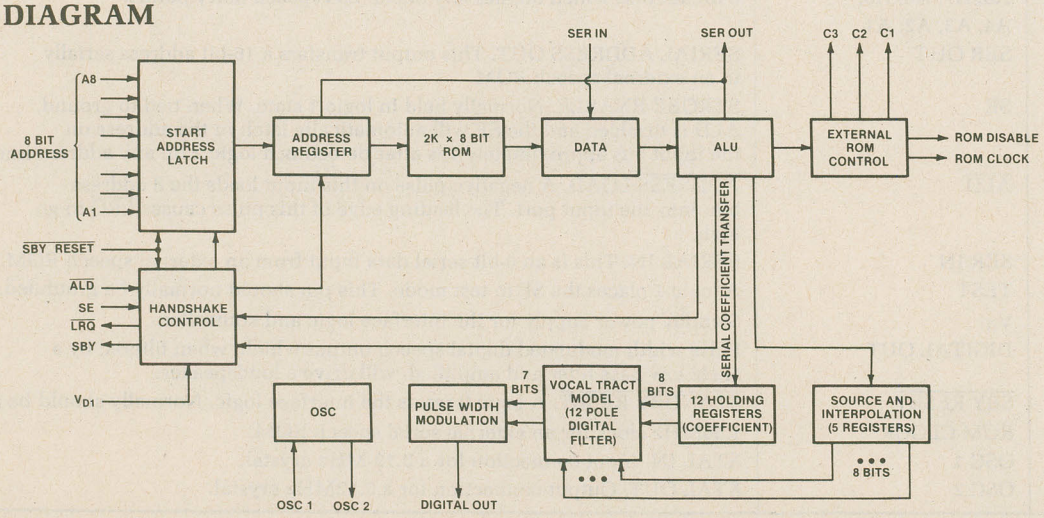
Outputs

SBY, DIGITAL OUT, C1, C2, C3, $\overline{LRQ}$, ROM DISABLE, ROM CLOCK, SER OUT
Logic 0, Vol [0.72mA(2 LS TTL Loads)] 0.6V
Logic 1, V_{OM} [-50μA (2 LS TTL Loads)] ..... V_{D1}V

AC CHARACTERISTICS

Clock Frequency (Crystal) ..... 3.120 MHz
$\overline{Reset}$, $\overline{SBY\ Reset}$ (t_{pw1}) ..... 100 μs
$\overline{ALD}$ (< 800ns) (t_{pw2}) ..... 200 ns
A1-A8 Set Up (t_{s2}) ..... 160 ns
A1-A8 Hold (t_{h2}) ..... 160 ns
$\overline{ALD}$ (≥ 800ns) (t_{pw3}) ..... 800 ns
A1-A8 Set Up (t_{83}) ..... 0 ns
A1-A8 Hold (t_{h3}) ..... 1200 ns
$\overline{LRQ}$ (t_{pd0}) ..... 640 ns
SBY (t_{pd0}) ..... 640 ns
Operating Temperature, T_A ..... 0 to 70°C

BLOCK DIAGRAM



SP0256 276-1783

HOUSE TALKING CLOCK SP0256 #2 VOCABULARY LIST

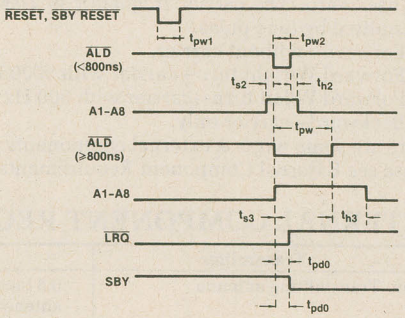
ADDRESS	WORD	ADDRESS	WORD
0	OH	18	EIGHTEEN
1	ONE	19	NINETEEN
2	TWO	20	TWENTY
3	THREE	21	THIRTY
4	FOUR	22	FORTY
5	FIVE	23	FIFTY
6	SIX	24	IT IS
7	SEVEN	25	A.M.
8	EIGHT	26	P.M.
9	NINE	27	HOUR
10	TEN	28	MINUTE
11	ELEVEN	29	HUNDRED HOUR
12	TWELVE	30	GOOD MORNING
13	THIRTEEN	31	ATTENTION PLEASE
14	FOURTEEN	32	PLEASE HURRY
15	FIFTEEN	33	MELODY A
16	SIXTEEN	34	MELODY B
17	SEVENTEEN	35	MELODY C

MELODY A: { 2/4 |3 1 2 5—| 5 2 3 1 |

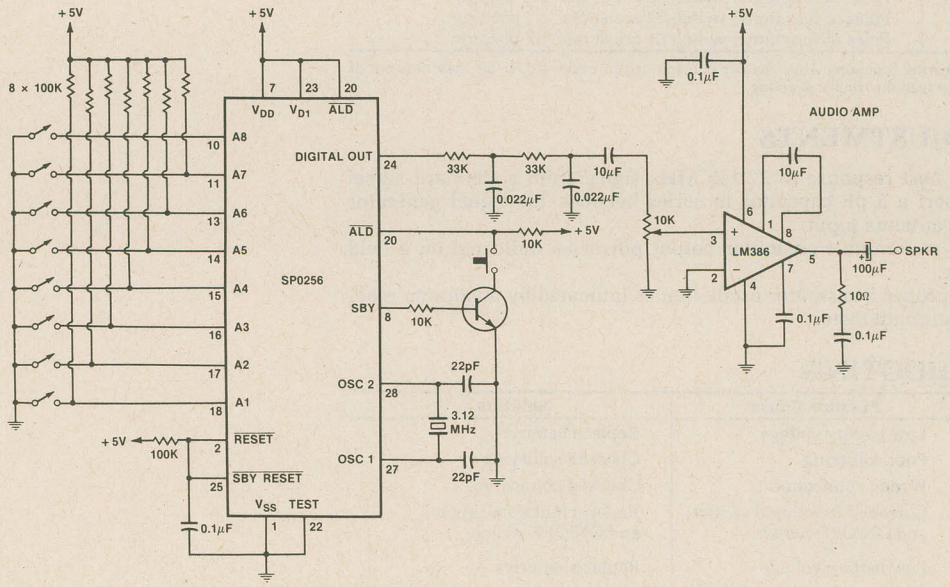
MELODY B: { 2/4 5 3 | 11 1234 | 5 5 5 0 | 3

MELODY C: { 2/4 1 5 | 1 53 | 5 23 | 1

TIMING DIAGRAM



TYPICAL APPLICATIONS



Stand Alone Configuration

277-1012 RADIO CONTROL ELECTRONIC KIT

GENERAL DESCRIPTION

This module was designed for radio control of cars, racers and boats. It can be operated in forward, forward with right turn, forward with left turn and backward. The carrier frequency is 27 MHz. The control commands are transmitted by tone pulse.

Forward—without carrier.
Forward W/right turn—carrier with 3000 Hz pulse modulation.
Forward W/left turn—carrier with 500 Hz pulse modulation.
Backward—carrier only.

There are some wires & external components that you need.
Please see External Component Requirements.

EXTERNAL COMPONENT REQUIREMENTS

Transmitter	Recommendations
Ant Transmitting antenna	0.5 meter (20 inch) length telescope antenna or steel wire.
S1 Functional switch for driving	Two poles, two throw switch (DPDT) (275-663)
S2 Functional switch for steering	Two poles, two throw switch with center off. (DPDT) (275-664)
Battery snap	For 006P 9V battery (270-325)
Receiver	**Recommendations**
Ant. Receiving antenna	0.3 meter (12 inch) length steel wire
M1 Steering motor	3V motor (Mabuchi motor RN-140-14180)
M2 Driving motor	3V motor (Mabuchi motor RE-280-2865)
S1 ON/OFF switch	2 poles, 2 throw slide switch (DPDT) (275-607)
Battery snap	For 006P 9V battery (270-325)
Battery holder	For two D cells 1.5V (270-386)

CONTROL INSTRUCTIONS

The receiver will respond to commands as follows:

Action	Command
Forward	ON/OFF switch of receiver is switched ON.
Forward and Right	Poles of functional switch S2 are at the "R" position
Forward and Left	Poles of functional switch S2 are at the "L" position
Backward	Poles of functional switch S1 are at the "B" position

Note: There are no steering functions while the car is being driven backward. If the system is out of command, please read the trouble shooting.

SIMPLE ADJUSTMENTS

1. Adjust L1 for best response to 27.145 MHz signal from a standard signal generator. Insert a 5 pF capacitor in series between the signal generator and receiver's antenna input.
2. Adjust L3 for maximum transmitter output power as indicated on a field strength meter.
3. Adjust L4 for proper transmitter oscillation as indicated by maximum reading on a field strength meter.

TROUBLESHOOTING

Trouble	Possible Cause	Solution
No function	Low battery voltage	Replace batteries
	Poor soldering	Checked soldering
	Wrong connection	Checked connection
	Corroded functional switch and ON/OFF switch.	Replace functional switch and ON/OFF switch
Insufficient control distance	Low battery voltage	Replace batteries
	Poor soldering for antenna	Checked soldering for antenna
	Length of antennas are not suitable	Replace with suitable antenna.

277-1012

ABSOLUTE MAXIMUM RATINGS

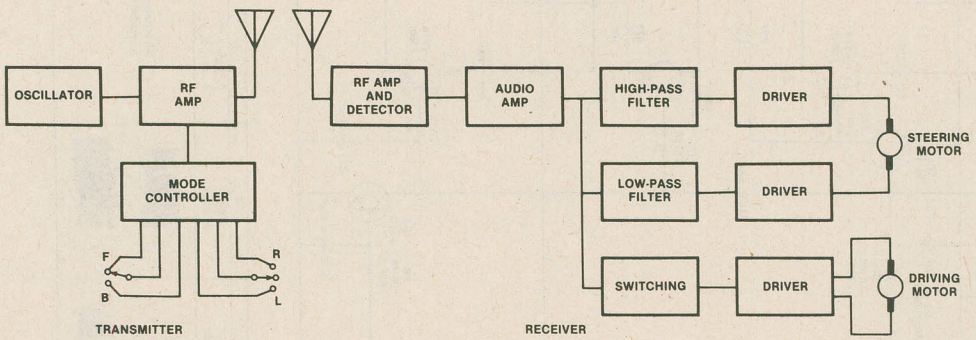
Transmitter

Frequency ..... 27.145 MHz
Current 17mA
Operating Voltage 9V
Battery Life ..... 10 Hours

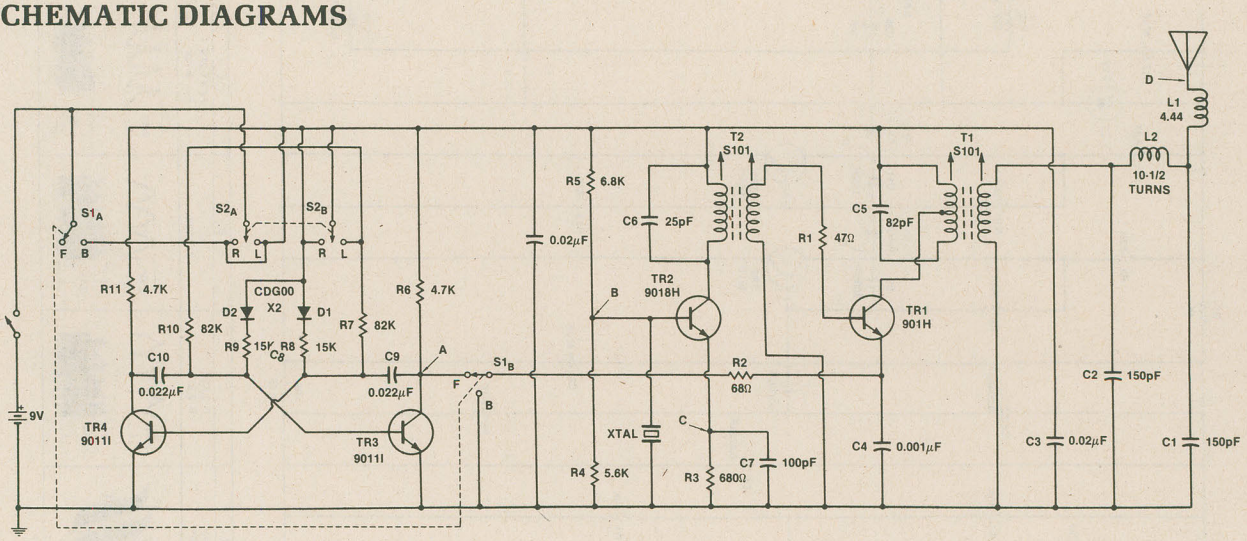
Receiver

Frequency ..... 27.145 MHz
Current 12mA
Operating Voltage 9V

BLOCK DIAGRAM



SCHEMATIC DIAGRAMS

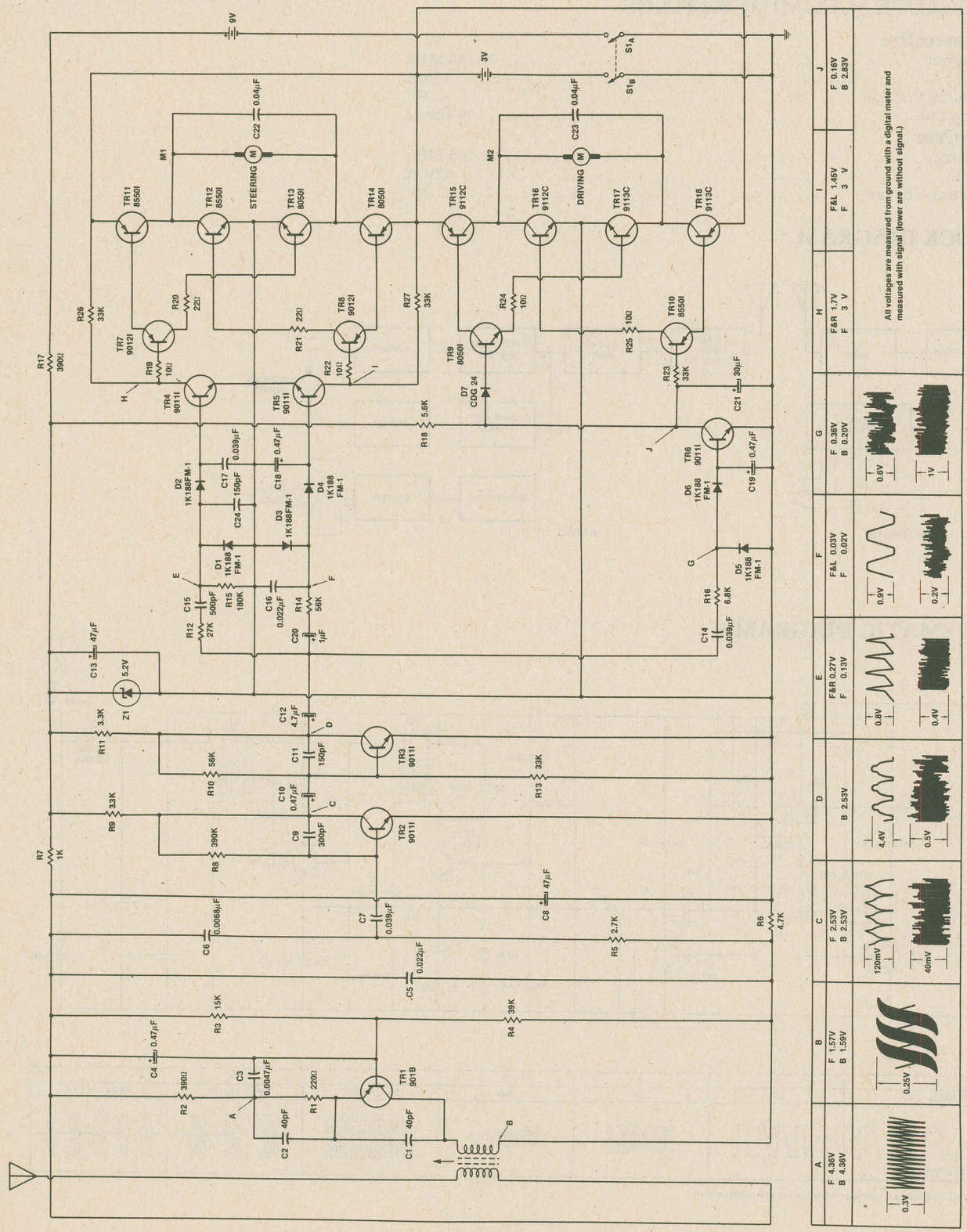


A		B	C	D		
VOLTAGE 2.9V	2.3V	2.2V	4.0V	B = CARRIER	F&L = 500Hz	F&R = 3000Hz
5V WAVEFORM	5V					

Note:All voltages are measured from ground with digital meter.

277-1012

SCHEMATIC DIAGRAMS (Cont'd)



IMPORTANT SUGGESTIONS ON THE USE AND REPLACEMENT OF TRANSISTORS

You can use various styles and sizes of transistors in any given circuit application, as long as the electrical characteristics of the device are within the required range of operation. Thus, a tab-type device can be used to replace a TO-3 or TO-66 case device; or a small epoxy-type device can be used in place of TO-5 or other size transistor.

Generally speaking, you must observe the following maximum characteristics of a transistor when contemplating substitution or selection:

Power dissipation
Maximum collector current
Maximum collector-to-emitter voltage
Maximum collector-to-base voltage
Maximum emitter-to-base voltage

Also, it is useful to consider the following characteristics for actual circuit operation:

Gain
Frequency limitations

Caution: It may be necessary in some cases to adjust bias values to achieve required operation. With tuned circuits, it is a good practice to check alignment after replacing any transistor.

When replacing power transistors, always check driver devices to be sure they are OK. Also, check other circuit components to be sure they were not shorted (or otherwise defective) when the original device failed. If you fail to correct such problems before applying power to the circuit once again, the replacement transistor could easily be permanently damaged. Be sure to use proper heat-sink precautions and use silicon grease to reduce the thermal resistance between the case of the transistor and the heat-sink.

Always observe temperature limitations as specified with transistor ratings.

It almost goes without saying, but let us remind you anyway—

Always observe voltage polarity with all semiconductor devices.

CROSS-REFERENCE/SUBSTITUTION LISTING

Most users of semiconductors realize that it is almost impossible to guarantee absolute equivalents (as in the case of tubes). Thus, the only way to create replacement or cross-reference listings is by carefully evaluating each characteristic of both devices (original transistor and the possible alternate). This is how the Technical Staff of Radio Shack went about preparing the following cross-reference/replacement lists.

IMPORTANT NOTE

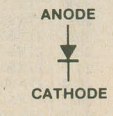
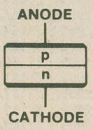
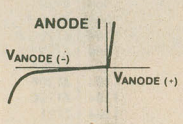
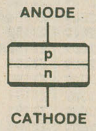
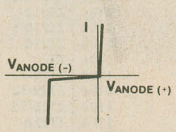
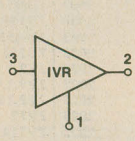
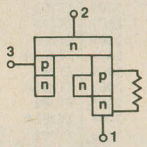
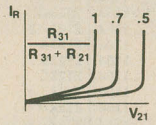
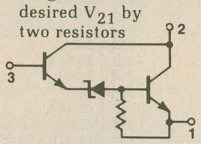
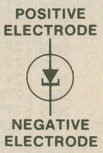
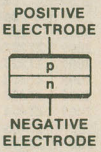
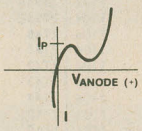
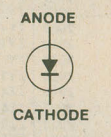
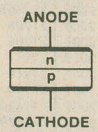
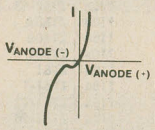
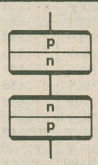
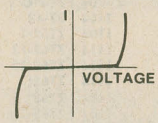
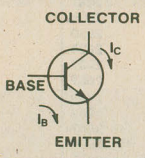
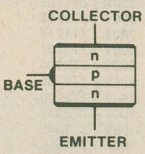
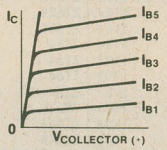
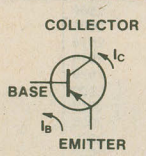
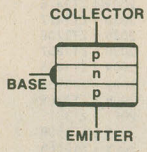
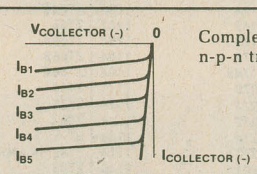
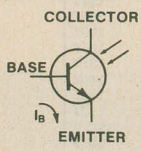
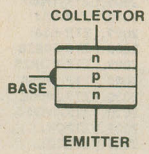
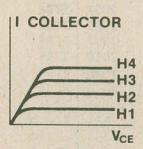
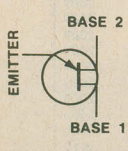
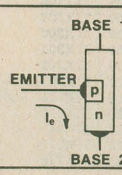
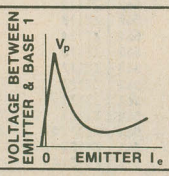
We caution you that in any cases the listed cross reference ARCHER device may be different in appearance, size or mounting style. Thus, before beginning replacement or installation procedues, check to be sure you have enough room for proper mounting.

Also, when making substitutions or replacements in radio or high frequency circuitry, it may be necessary to realign tunable circuit elements. This is true even when making **exact** replacements (junction capacitances normally vary between devices even from the same production run).

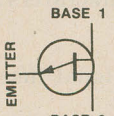
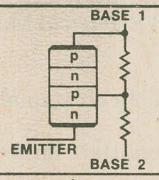
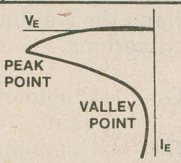
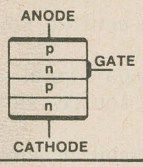
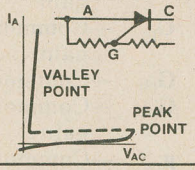
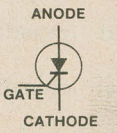
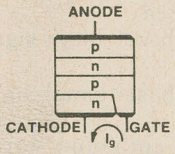
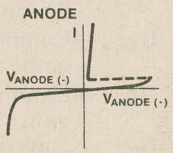
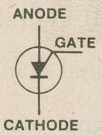
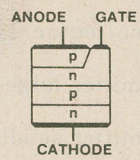
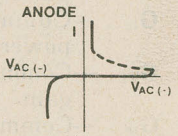
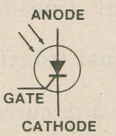
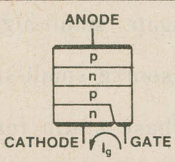
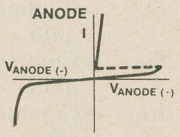
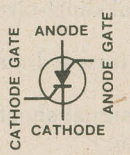
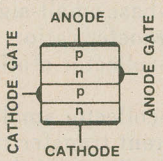
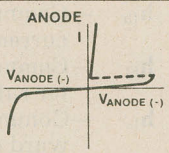
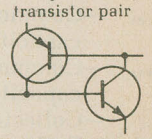
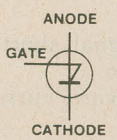
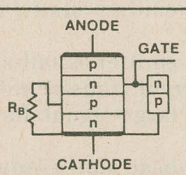
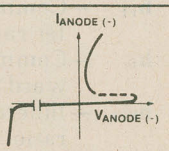
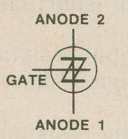
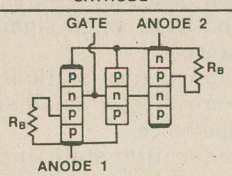
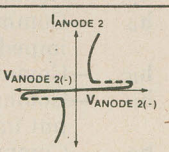
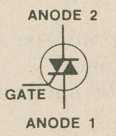
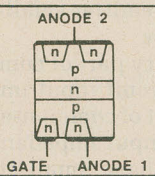
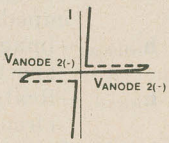
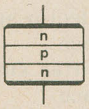
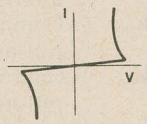
Information contained in this guide is based on the latest available data and is believed to be accurate. Every care has been taken to assure technical accuracy. However, Radio Shack does not assume responsibility for any contingencies of the use of this information. Nor does Radio Shack assume any responsibility for any infringements of patents or other rights of third parties which may result from its use.

When you are looking for a specific number and it does not show up in the following listing—refer to the technical data provided for our line of ARCHER devices. With this information you probably will be able to make a suitable substitution.

MAJOR SEMICONDUCTOR COMPONENTS

NAME OF DEVICE	CIRCUIT SYMBOL	COMMONLY USED JUNCTION SCHEMATIC	ELECTRICAL CHARACTERISTICS		MAX RATINGS AVAILABLE	MAJOR APPLICATIONS	ROUGHLY ANALOGOUS TO:
Diode or Rectifier				Conducts easily in one direction, blocks in the other	1500 Amps 3000 Volts	Rectification Blocking Detecting Steering	Check valve Diode tube Gas diode
Avalanche (Zener) Diode				Constant voltage characteristic in negative quadrant	22 Volts 1 Watt	Regulation Reference Clipping	V-R tube
Integrated Voltage Regulator (IVR)				Programmed to desired V_{21} by two resistors		40 Volts 100 mA 0.4 Watts	Shunt voltage regulator Reference element Error modifier Level sensing Level shifting	Avalanche Diode
Tunnel Diode				Displays negative resistance when current exceeds peak point current I_p	Peak point current = 100 mA Resistive cutoff freq. = 40 Gc	UHF converter Logic circuits Microwave circuits Level sensing	None
Back Diode				Similar characteristics to conventional diode except very low forward voltage drop	5 mA 400 mV	Microwave mixers and low power oscillators	None
Thyrector				Rapidly increasing current above rated voltage in either direction	70 A peak pulse (2" Sq. cell)	Transient voltage suppression and arc suppression	Thyrite Two avalanche diodes in inverse-series connection
n-p-n Transistor				Constant collector current for given base drive	300 Volts 25 Watts	Amplification Switching Oscillation	Pentode Tube
p-n-p Transistor				Complement to n-p-n transistor	75 Volts 25 Watts	Amplification Switching Oscillation	None
Photo Transistor				Incident light acts as base current of the photo transistor	45 Volts 0.25 Amps 0.6 Watts	Tape readers Card readers Position sensor Tachometers	None
Unijunction Transistor (UJT)				Unijunction emitter blocks until its voltage reaches V_p; then conducts	35 Volts 0.450 Watts	Interval timing Oscillation Level Detector SCR Trigger	None

MAJOR SEMICONDUCTOR COMPONENTS

NAME OF DEVICE	CIRCUIT SYMBOL	COMMONLY USED JUNCTION SCHEMATIC	ELECTRICAL CHARACTERISTICS		MAX RATINGS AVAILABLE	MAJOR APPLICATIONS	ROUGHLY ANALOGOUS TO:
Complementary Unijunction Transistor (CUJT)				Functional complement to UJT	30 Volts 0.30 Watts 0.15 Amps	High stability timers Oscillators and level detectors	None
Programmable Unijunction Transistor (PUT)				Programmed by two resistors for V_p, I_p, I_v. Function equivalent to normal UJT.	40 Volts 0.30 Watts 0.15 Amps	Low cost timers and oscillators Long period timers SCR trigger Level detector	UJT
Silicon Controlled Rectifier (SCR)				With anode voltage (+), SCR can be triggered by I_g, remaining in conduction until anode I is reduced to zero	1000 Amps 1800 Volts	Power switching Phase control Inverters Choppers	Gas thyratron or ignitron
Complementary Silicon Controlled Rectifier (CSCR)				Polarity complement to SCR	50 Volts 0.25 Amps 0.45 Watts	Ring counters Low speed logic Lamp driver	None
Light Activated SCR* (LASCR)				Operates similar to SCR, except can also be triggered into conduction by light falling on junctions	1.6 Amps 200 Volts	Relay Replacement Position controls Photoelectric applications Slave flashes	None
Silicon Controlled Switch* (SCS)				Operates similar to SCR except can also be triggered on by a negative signal on anode-gate. Also several other specialized modes of operation	100 Volts 200 mA	Logic applications Counters Nixie drivers Lamp drivers	Complementary transistor pair 
Silicon Unilateral Switch (SUS)				Similar to SCS but zener added to anode gate to trigger device into conduction at ~ 8 volts. Can also be triggered by negative pulse at gate lead.	0.350 Watts 0.200 Amps 10 Volts	Switching Circuits Counters SCR Trigger Oscillator	Shockley or 4-layer diode
Silicon Bilateral Switch (SBS)				Symmetrical bilateral version of the SUS. Breaks down in both directions as SUS does in forward.	0.350 Watts 0.200 Amps 10 Volts	Switching Circuits Counters TRIAC Phase Control	Two inverse Schockley diodes
Triac				Operates similar to SCR except can be triggered into conduction in either direction by (+) or (-) gate signal	25 Amps 500 Volts	AC switching Phase control Relay replacement	Two SCR's in inverse parallel
Diac Trigger				When voltage reaches trigger level (about 35 volts), abruptly switches down about 10 volts.	40 Volts 2 Amps peak	Triac and SCR trigger Oscillator	Neon lamp

*Light Activated SCS also available.

GLOSSARY OF WORDS, SYMBOLS AND ABBREVIATIONS

The following letter symbols and abbreviations are recommended by the Joint Electron Device Engineering Council (JEDEC) of the Electronic Industries Association (EIA) and the National Electrical Manufacturers Association (NEMA) for use in semiconductor device data sheets and specifications.

A, a —Anode
B, b —Base
$\mathbf{b_{fs}}$ —Common-source small-signal forward transfer susceptance
$\mathbf{b_{is}}$ —Common-source small-signal input susceptance
$\mathbf{b_{os}}$ —Common-source small-signal output susceptance
$\mathbf{b_{rs}}$ —Common-source small-signal reverse transfer susceptance
C, c —Collector
$\mathbf{C_{cb}}$ —Collector-base interterminal capacitance
$\mathbf{C_{ce}}$ —Collector-emitter interterminal capacitance
$\mathbf{C_{ds}}$ —Drain-source capacitance
$\mathbf{C_{du}}$ —Drain-substrate capacitance
$\mathbf{C_{eb}}$ —Emitter-base interterminal capacitance
$\mathbf{C_{ibo}}$ —Common-base open-circuit input capacitance
$\mathbf{C_{ibs}}$ —Common-base short-circuit input capacitance
$\mathbf{C_{ieo}}$ —Common-emitter open-circuit input capacitance
$\mathbf{C_{ies}}$ —Common-emitter short-circuit input capacitance
$\mathbf{C_{iss}}$ —Common-source short-circuit input capacitance
$\mathbf{C_{obo}}$ —Common-base open-circuit output capacitance
$\mathbf{C_{obs}}$ —Common-base short-circuit output capacitance
$\mathbf{C_{oeo}}$ —Common-emitter open-circuit output capacitance
$\mathbf{C_{oes}}$ —Common-emitter short-circuit output capacitance
$\mathbf{C_{oss}}$ —Common-source short-circuit output capacitance
$\mathbf{C_{rbs}}$ —Common-base short-circuit reverse transfer capacitance
$\mathbf{C_{rcs}}$ —Common-collector short-circuit reverse transfer capacitance
$\mathbf{C_{res}}$ —Common-emitter short-circuit reverse transfer capacitance
$\mathbf{C_{rss}}$ —Common-source short-circuit reverse transfer capacitance
$\mathbf{C_{tc}}$ —Collector depletion-layer capacitance
$\mathbf{C_{te}}$ —Emitter depletion-layer capacitance
D, d —Drain
E, e —Emitter
η —Intrinsic standoff ratio
$\mathbf{f_{hfb}}$ —Common-base small-signal short-circuit forward current transfer ratio cutoff frequency
$\mathbf{f_{hfc}}$ —Common-collector small-signal short-circuit forward current transfer ratio cutoff frequency
$\mathbf{f_{hfe}}$ —Common-emitter small-signal short-circuit forward current transfer ratio cutoff frequency
$\mathbf{f_{max}}$ —Maximum frequency of oscillation
$\mathbf{F_T}$ —Transition frequency (frequency at which common-emitter small-signal forward current transfer ratio extrapolates to unity)
G, g —Gate
$\mathbf{g_{fs}}$ —Common-source small-signal forward transfer conductance
$\mathbf{g_{is}}$ —Common-source small-signal input conductance
$\mathbf{g_{MB}}$ —Common-base static transconductance
$\mathbf{g_{MC}}$ —Common-collector static transconductance
$\mathbf{g_{ME}}$ —Common-emitter static transconductance
$\mathbf{g_{os}}$ —Common-source small-signal output conductance
$\mathbf{G_{PB}}$ —Common-base large-signal insertion power gain
$\mathbf{G_{pb}}$ —Common-base small-signal insertion power gain
$\mathbf{G_{PC}}$ —Common-collector large-signal insertion power gain
$\mathbf{G_{pc}}$ —Common-collector small-signal insertion power gain
$\mathbf{G_{PE}}$ —Common-emitter large-signal insertion power gain
$\mathbf{G_{pe}}$ —Common-emitter small-signal insertion power gain
$\mathbf{G_{pg}}$ —Common-gate small-signal insertion power gain
$\mathbf{G_{ps}}$ —Common-source small-signal insertion power gain
$\mathbf{g_{rs}}$ —Common-source small-signal reverse transfer conductance
$\mathbf{G_{TB}}$ —Common-base large-signal transducer power gain
$\mathbf{G_{tb}}$ —Common-base small-signal transducer power gain
$\mathbf{G_{TC}}$ —Common-collector large-signal transducer power gain
$\mathbf{G_{tc}}$ —Common-collector small-signal transducer power gain
$\mathbf{G_{TE}}$ —Common-emitter large-signal transducer power gain
$\mathbf{G_{te}}$ —Common-emitter small-signal transducer power gain
$\mathbf{G_{tg}}$ —Common-gate small-signal transducer power gain
$\mathbf{G_{ts}}$ —Common-source small-signal transducer power gain
$\mathbf{h_{FB}}$ —Common-base static forward current transfer ratio
$\mathbf{h_{fb}}$ —Common-base small-signal short-circuit forward current transfer ratio
$\mathbf{h_{FC}}$ —Common-collector static forward current transfer ratio
$\mathbf{h_{fc}}$ —Common-collector small-signal short-circuit forward current transfer ratio
$\mathbf{h_{FE}}$ —Common-emitter static forward current transfer ratio
$\mathbf{h_{fe}}$ —Common-emitter small-signal short-circuit forward current transfer ratio
$\mathbf{h_{FEL}}$ —Inherent large-signal forward current transfer ratio
$\mathbf{h_{IB}}$ —Common-base static input resistance
$\mathbf{h_{ib}}$ —Common-base small-signal short-circuit input impedance
$\mathbf{h_{IC}}$ —Common-collector static input resistance
$\mathbf{h_{ic}}$ —Common-collector small-signal short-circuit input impedance
$\mathbf{h_{IE}}$ —Common-emitter static input resistance
$\mathbf{h_{ie}}$ —Common-emitter small-signal short-circuit input impedance
$\mathbf{h_{ie(imag)}}$ —Imaginary part of common-emitter small-signal short-circuit input impedance
$\mathbf{h_{ie(real)}}$ —Real part of common-emitter small-signal short-circuit input impedance
$\mathbf{h_{ob}}$ —Common-base small-signal open-circuit output admittance
$\mathbf{h_{oc}}$ —Common-collector small-signal open-circuit output admittance
$\mathbf{h_{oe}}$ —Common-emitter small-signal open-circuit output admittance
$\mathbf{h_{oe(imag)}}$ —Imaginary part of common-emitter small-signal open-circuit output admittance

$h_{oe(real)}$ —Real part of common-emitter small-signal open-circuit output admittance
h_{rb} —Common-base small-signal open-circuit reverse voltage transfer ratio
h_{rc} —Common-collector small-signal open-circuit reverse voltage transfer ratio
h_{re} —Common-emitter small-signal open-circuit reverse voltage transfer ratio
I_B —Base-terminal dc current
I_b —Alternating component (rms value) of base-terminal current
i_B —Instantaneous total value of base-terminal current
I_{BEV} —Base cutoff current, dc
$I_{B2(mod)}$ —Interbase modulated current
I_C —Collector-terminal dc current
I_c —Alternating component (rms value) of collector-terminal current
i_C —Instantaneous total value of collector-terminal current
I_{CBO} —Collector cutoff current (dc), emitter open
I_{CEO} —Collector cutoff current (dc), base open
I_{CER} —Collector cutoff current (dc), specified resistance between base and emitter
I_{CES} —Collector cutoff current (dc), base shorted to emitter
I_{CEV} —Collector cutoff current (dc), specified voltage between base and emitter
I_{CEX} —Collector cutoff current (dc), specified circuit between base and emitter
I_D —Drain current, dc
$I_{D(off)}$ —Drain cutoff current
$I_{D(on)}$ —On-state drain current
I_{DSS} —Zero-gate-voltage drain current
I_E —Emitter-terminal dc current
I_e —Alternating component (rms value) of emitter-terminal current
i_E —Instantaneous total value of emitter-terminal current
I_{EBO} —Emitter cutoff current (dc), collector open
I_{EB20} —Emitter reverse current
$I_{EC(ofs)}$ —Emitter-collector offset current
I_{ECS} —Emitter cutoff current (dc), base short-circuited to collector
$I_{E1E2(off)}$ —Emitter cutoff current
I_F —For voltage-regulator and voltage-reference diodes: dc forward current. For signal diodes and rectifier diodes: dc forward current (no alternating component)
I_f —Alternating component of forward current (rms value)
i_F —Instantaneous total forward current
$I_{F(AV)}$ —Forward current, dc (with alternating component)
I_{FM} —Maximum (peak) total forward current
$I_{F(OV)}$ —Forward current, overload
I_{FRM} —Maximum (peak) forward current, repetitive
$I_{F(RMS)}$ —Total rms forward current
I_{FSM} —Maximum (peak) forward current, surge
I_G —Gate current, dc
I_{GF} —Forward gate current
I_{GR} —Reverse gate current
I_{GSS} —Reverse gate current, drain short-circuited to source
I_{GSSF} —Forward gate current, drain short-circuited to source
I_{GSSR} —Reverse gate current, drain short-circuited to source
I_I —Inflection-point current
$Im(h_{ie})$—Imaginary part of common-emitter small-signal short-circuit input impedance
$Im(h_{oe})$—Imaginary part of common-emitter small-signal open-circuit output admittance
I_O —Average forward current, 180° conduction angle, 60-Hz half sine wave
I_P —Peak-point current
I_R —For voltage-regulator and voltage-reference diodes: dc reverse current. For signal diodes and rectifier diodes: dc reverse current (no alternating component)
I_r —Alternating component of reverse current (rms value)
i_R —Instantaneous total reverse current
$I_{R(AV)}$ —Reverse current, dc (with alternating component)
I_{RM} —Maximum (peak) total reverse current
I_{RRM} —Maximum (peak) reverse current, repetitive
$I_{R(RMS)}$ —Total rms reverse current
I_{RSM} —Maximum (peak) surge reverse current
I_S —Source current, dc
I_{SDS} —Zero-gate-voltage source current
$I_{S(off)}$ —Source cutoff current
I_V —Valley-point current
I_Z —Regulator current, reference current (dc)
I_{ZK} —Regulator current, reference current (dc near breakdown knee)
I_{ZM} —Regulator current, reference current (dc maximum rated current)
K, k —Cathode
L_c —Conversion loss
M —Figure of merit
NF_o —Overall noise figure
NR_o —Output noise ratio
P_{BE} —Power input (dc) to base, common emitter
p_{BE} —Instantaneous total power input to base, common emitter
P_{CB} —Power input (dc) to collector, common base
p_{CB} —Instantaneous total power input to collector, common base
P_{CE} —Power input (dc) to collector, common emitter
p_{CE} —Instantaneous total power input to collector, common emitter
P_{EB} —Power input (dc) to emitter, common base
p_{EB} —Instantaneous total power input to emitter, common base
P_F —Forward power dissipation, dc (no alternating component)
p_F —Instantaneous total forward power dissipation
$P_{F(AV)}$—Forward power dissipation, dc (with alternating component)
P_{FM} —Maximum (peak) total forward power dissipation
P_{IB} —Common-base large-signal input power
p_{ib} —Common-base small-signal input power
P_{IC} —Common-collector large-signal input power
p_{ic} —Common-collector small-signal input power
P_{IE} —Common-emitter large-signal input power
p_{ie} —Common-emitter small-signal input power
P_{OB} —Common-base large-signal output power
p_{ob} —Common-base small-signal output power
P_{OC} —Common-collector large-signal output power
p_{oc} —Common-collector small-signal output power
P_{OE} —Common-emitter large-signal output power
p_{oe} —Common-emitter small-signal output power
P_R —Reverse power dissipation, dc (no alternating component)
p_R —Instantaneous total reverse power dissipation
$P_{R(AV)}$—Reverse power dissipation, dc (with alternating component)

P_{RM} —Maximum (peak) total reverse power dissipation
P_T —Total nonreactive power input to all terminals
p_T —Nonreactive power input, instantaneous total, to all terminals
Q_S —Stored charge
r_{BB} —Interbase resistance
$r_b'C_c$ —Collector-base time constant
$r_{CE(sat)}$ —Saturation resistance, collector-to-emitter
$r_{DS(on)}$ —Static drain-source on-state resistance
$r_{ds(on)}$ —Small-signal drain-source on-state resistance
$Re(h_{ie})$—Real part of common-emitter small-signal short-circuit input impedance
$Re(h_{oe})$—Real part of common-emitter small-signal open-circuit output admittance
$r_{e1e2(on)}$—Small-signal emitter-emitter on-state resistance
r_i —Dynamic resistance at inflection point
R_θ —Thermal resistance
$R_{\theta CA}$ —Thermal resistance, case to ambient
$R_{\theta JA}$ —Thermal resistance, junction to ambient
$R_{\theta JC}$ —Thermal resistance, junction to case
S, s —Source
T_A —Ambient temperature or free-air temperature
T_C —Case temperature
t_d —Delay time
$t_{d(off)}$ —Turn-off delay time
$t_{d(on)}$ —Turn-on delay time
t_f —Fall time
t_{fr} —Forward recovery time
T_j —Junction temperature
t_{off} —Turn-off time
t_{on} —Turn-on time
t_p —Pulse time
t_r —Rise time
t_{rr} —Reverse recovery time
t_s —Storage time
TSS —Tangential signal sensitivity
T_{stg} —Storage temperature
t_w —Pulse average time
U, u —Bulk (substrate)
V_{BB} —Base supply voltage (dc)
V_{BC} —Average or dc voltage, base to collector
v_{bc} —Instantaneous value of alternating component of base-collector voltage
V_{BE} —Average or dc voltage, base to emitter
v_{be} —Instantaneous value of alternating component of base-emitter voltage
$V_{(BR)}$ —Breakdown voltage (dc)
$v_{(BR)}$ —Breakdown voltage (instantaneous total)
$V_{(BR)CBO}$ —Collector-base breakdown voltage, emitter open
$V_{(BR)CEO}$ —Collector-emitter breakdown voltage, base open
$V_{(BR)CER}$ —Collector-emitter breakown voltage, resistance between base and emitter
$V_{(BR)CES}$ —Collector-emitter breakdown voltage, base shorted to emitter
$V_{(BR)CEV}$ —Collector-emitter breakdown voltage, specified voltage between base and emitter
$V_{(BR)CEX}$ —Collector-emitter breakdown voltage, specified circuit between base and emitter
$V_{(BR)EBO}$ —Emitter-base breakdown voltage, collector open
$V_{(BR)ECO}$ —Emitter-collector breakdown voltage, base
$V_{(BR)E1E2}$ —Emitter-emitter breakdown voltage
$V_{(BR)GSS}$ —Gate-source breakdown voltage
$V_{(BR)GSSF}$—Forward gate-source breakdown voltage
$V_{(BR)GSSR}$—Reverse gate-source breakdown voltage
V_{B2B1} —Interbase voltage
V_{CB} —Average or dc voltage, collector to base
v_{cb} —Instantaneous value of alternating component of collector-base voltage
$V_{CB(fl)}$ —Collector-base dc open-circuit voltage (floating potential)
V_{CBO} —Collector-base voltage, dc, emitter open
V_{CC} —Collector supply voltage (dc)
V_{CE} —Average or dc voltage, collector to emitter
v_{ce} —Instantaneous value of alternating component of collector-emitter voltage
$V_{CE(fl)}$—Collector-emitter dc open-circuit voltage (floating potential)
V_{CEO} —Collector-emitter voltage (dc), base open
$V_{CE(ofs)}$ —Collector-emitter offset voltage
V_{CER} —Collector-emitter voltage (dc), resistance between base and emitter
V_{CES} —Collector-emitter voltage (dc), base shorted to emitter
$V_{CE(sat)}$ —Collector-emitter dc saturation voltage
V_{CEV} —Collector-emitter voltage (dc), specified voltage between base and emitter
V_{CEX} —Collector-emitter voltage (dc), specified circuit between base and emitter
V_{DD} —Drain supply voltage (dc)
V_{DG} —Drain-gate voltage
V_{DS} —Drain-source voltage
$V_{DS(on)}$ —Drain-source on-state voltage
V_{DU} —Drain-substrate voltage
V_{EB} —Average or dc voltage, emitter to base
v_{eb} —Instantaneous value of alternating component of emitter-base voltage
$V_{EB(fl)}$—Emitter-base dc open-circuit voltage (floating potential)
V_{EBO} —Emitter-base voltage (dc), collector open
$V_{EB1(sat)}$—Emitter saturation voltage
V_{EC} —Average or dc voltage, emitter to collector
v_{ec} —Instantaneous value of alternating component of emitter-collector voltage
$V_{EC(fl)}$—Emitter-collector dc open-circuit voltage (floating potential)
$V_{EC(ofs)}$ —Emitter-collector offset voltage
V_{EE} —Emitter supply voltage (dc)
V_F —For voltage-regulator and voltage-reference diodes: dc forward voltage. For signal diodes and rectifier diodes: dc forward voltage (no alternating component)
V_f —Alternating component of forward voltage (rms value)
V_F —Instantaneous total forward voltage
$V_{F(AV)}$—Forward voltage, dc (with alternating component)
V_{FM} —Maximum (peak) total forward voltage
$V_{F(RMS)}$—Total rms forward voltage
V_{GG} —Gate supply voltage (dc)
V_{GS} —Gate-source voltage
V_{GSF} —Forward gate-source voltage
$V_{GS(off)}$ —Gate-source cutoff voltage
V_{GSR} —Reverse gate-source voltage
$V_{GS(th)}$ —Gate-source threshold voltage
V_{GU} —Gate-substrate voltage
V_I —Inflection-point voltage
V_{OB1} —Base-1 peak voltage
V_P —Peak-point voltage
V_{PP} —Projected peak-point voltage
V_R —For voltage-regulator and voltage-reference diodes: dc reverse voltage. For signal diodes and rectifier diodes: dc reverse voltage (no alternating component)
V_r —Alternating component of reverse voltage (rms value)

v_R —Instantaneous total reverse voltage
$V_{R(AV)}$ —Reverse voltage, dc (with alternating component)
V_{RM} —Maximum (peak) total reverse voltage
V_{RRM} —Repetitive peak reverse voltage
$V_{R(RMS)}$—Total rms reverse voltage
V_{RSM} —Nonrepetitive peak reverse voltage
V_{RT} —Reach-through voltage
V_{RWM}—Working peak reverse voltage
V_{SS} —Source supply voltage (dc)
V_{SU} —Source-substrate voltage
$V_{(TO)}$ —Threshold voltage
V_V —Valley-point voltage
V_Z —Regulator voltage, reference voltage (dc)
V_{ZM} —Regulator voltage, reference voltage (dc at maximum rated current)
y_{fb} —Common-base small-signal short-circuit forward transfer admittance
y_{fc} —Common-collector small-signal short-circuit forward transfer admittance
y_{fe} —Common-emitter small-signal short-circuit forward transfer admittance
y_{fs} —Common-source small-signal short-circuit forward transfer admittance
$y_{fs(imag)}$—Common-source small-signal forward transfer susceptance
$y_{fs(real)}$ —Common-source small-signal forward transfer conductance
y_{ib} —Common-base small-signal short-circuit input admittance
y_{ic} —Common-collector small-signal short-circuit input admittance
y_{ie} —Common-emitter small-signal short-circuit input admittance
$y_{ie(imag)}$—Imaginary part of small-signal short-circuit input admittance (common-emitter)
$y_{ie(real)}$ —Real part of small-signal short-circuit input admittance (common-emitter)
y_{is} —Common-source small-signal short-circuit input admittance
$y_{is(imag)}$—Common-source small-signal input susceptance
$y_{is(real)}$—Common-source small-signal input conductance
y_{ob} —Common-base small-signal short-circuit output admittance
y_{oc} —Common-collector small-signal short-circuit output admittance
y_{oe} —Common-emitter small-signal short-circuit output admittance
$y_{oe(imag)}$—Imaginary part of small-signal short-circuit output admittance (common-emitter)
$y_{oe(real)}$ —Real part of small-signal short-circuit output admittance (common-emitter)
y_{os} —Common-source small-signal short-circuit output admittance
$y_{os(imag)}$—Common-source small-signal output susceptance
$y_{os(real)}$ —Common-source small-signal output conductance
y_{rb} —Common-base small-signal short-circuit reverse transfer admittance
y_{rc} —Common-collector small-signal short-circuit reverse transfer admittance
y_{re} —Common-emitter small-signal short-circuit reverse transfer admittance
y_{rs} —Common-source small-signal short-circuit reverse transfer admittance
$y_{rs(imag)}$—Common-source small-signal reverse transfer susceptance
$y_{rs(real)}$ —Common-source small-signal reverse transfer conductance
z_{if} —Intermediate-frequency impedance
z_m —Modulator-frequency load impedance
z_{rf} —Radio-frequency impedance
$Z_{\theta JA(t)}$—Junction-to-ambient transient thermal impedance
$Z_{\theta JC(t)}$—Junction-to-case transient thermal impedance
$Z_{\theta(t)}$ —Transient thermal impedance
z_v —Video impedance
z_z —Regulator impedance, reference impedance (small-signal at I_z)
z_{zk} —Regulator impedance, reference impedance (small-signal at I_{ZK})
z_{zm} —Regulator impedance, reference impedance (small-signal at I_{ZM})

PREFIX AND MANUFACTURER IDENTIFICATION

PREFIX	MANUFACTURER
BA	Rohm
CEX	Control Electronics
DAC	National Semiconductor
FND	Fairchild
FRL	Litronix
ICM	Intersil
LF	National Semiconductor
LM	National Semiconductor
MA	National Semiconductor
MC	Motorola
MJ	Motorola
MM	National Semiconductor, Motorola or Teledyne
MOC	Motorola
MPS	Motorola
MRF	Motorola
MU	Motorola
MV	General Instrument
NE	Signetics
NSM	National Semiconductor
PCIM	PC International
S	American Micro Systems
SAD	Reticon
SE	Signetics
SEL	Sanken
SCS	Spectronics
SLP	Sanyo
SN	Texas Instrument
TA	Toshiba
TIL	Texas Instrument
TIP	Motorola
TLO	Texas Instrument
TL	Texas Instrument
TLG	Toshiba
TLR	Toshiba
VN	Siliconix
XC	Xciton

GENERIC PART NUMBER PREFIX CODE

AD	Analog To Digital	DA	Digital To Analog	LM	Linear Monolithic
AH	Analog Hybrid	DM	Digital Monolithic	MM	MOS Monolithic
AM	Analog Monolithic	LF	Linear FET	TBA	Linear Monolithic
CD	CMOS Digital	LH	Linear Hybrid		

ALPHABETICAL/NUMERICAL INDEX

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